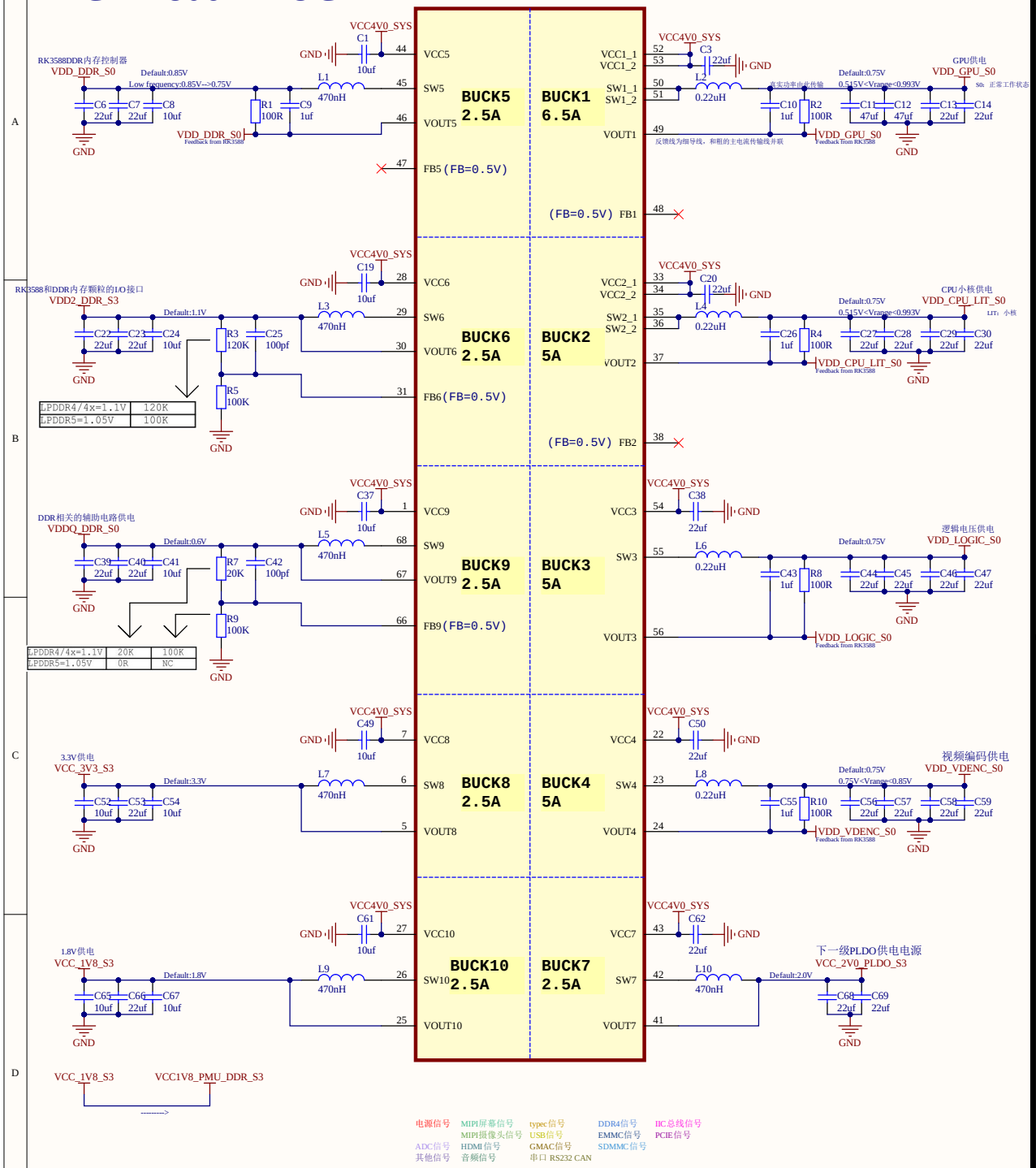
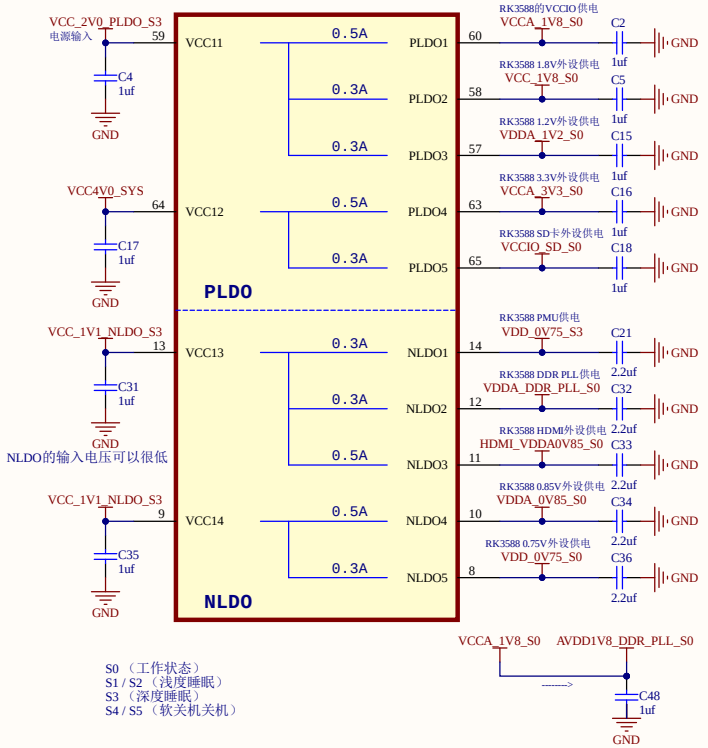
PMIC RK806-1 BUCK

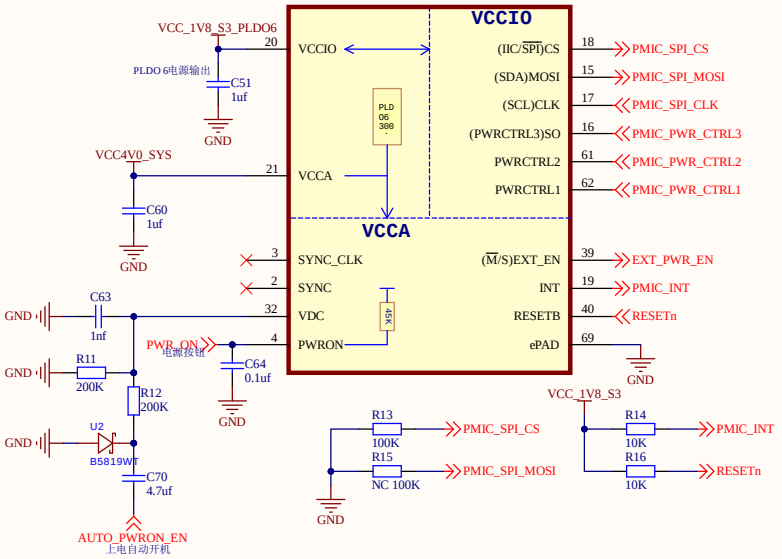


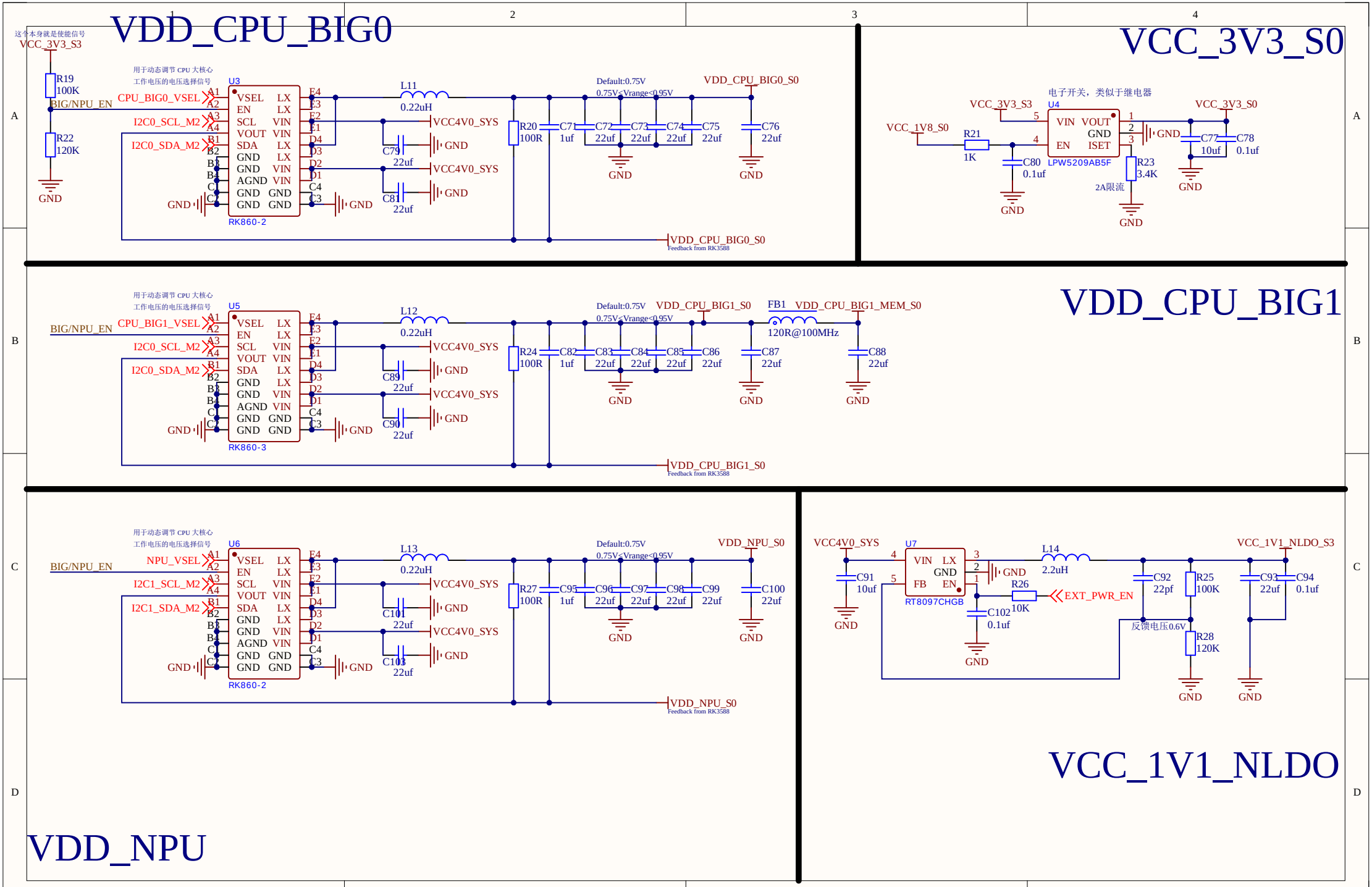
电源信号 MIPI屏幕信号 typec信号 DDR4信号 IIC总线信号
ADC信号 MIPI摄像头信号 USB信号 EMMC信号 PCIE信号
HDMI信号 GMAC信号 SDMMC信号
其他信号 音频信号 串口 RS232 CAN

PMIC RK806-1 LDO

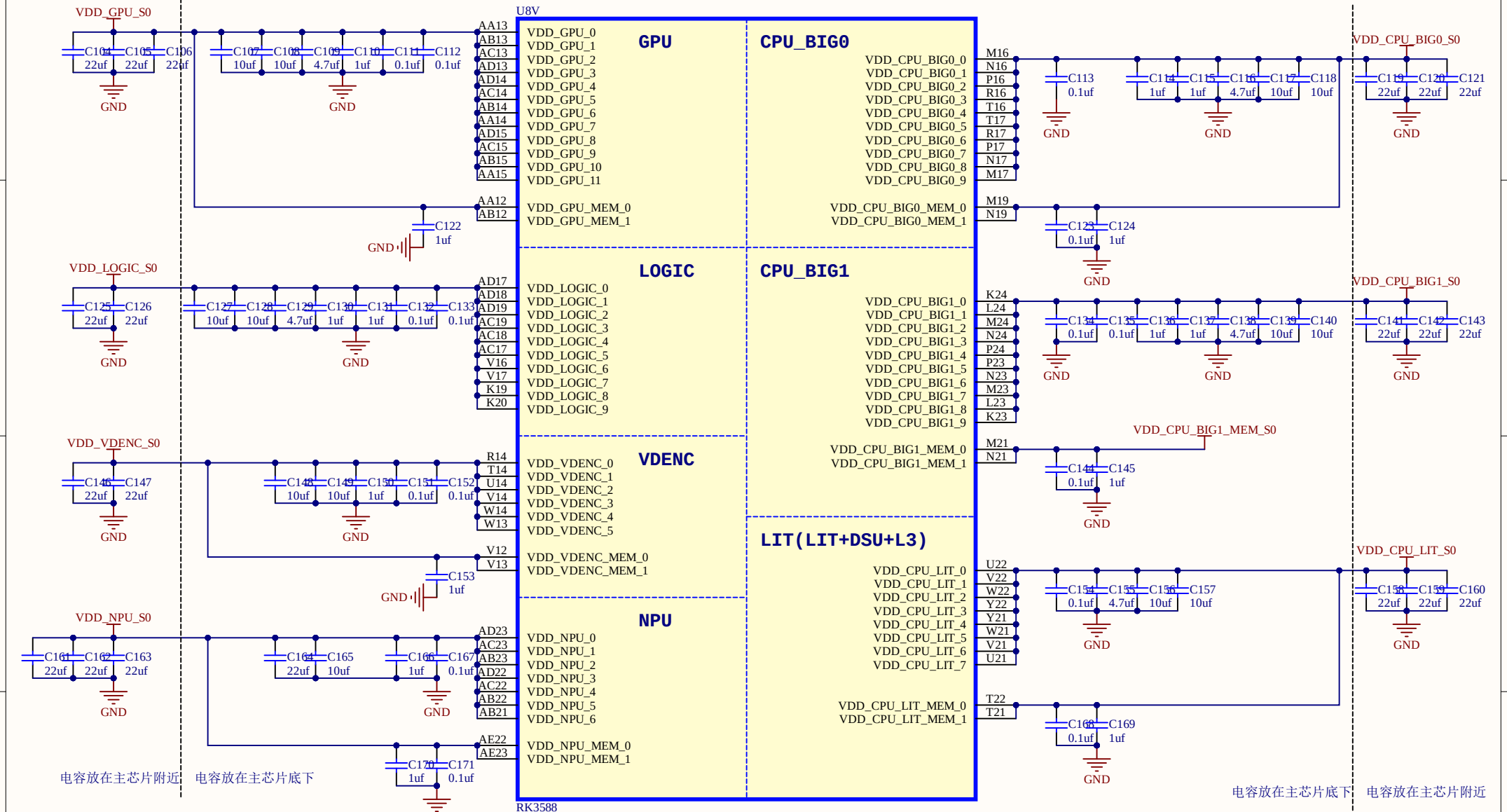


PMIC RK806-1 LDO

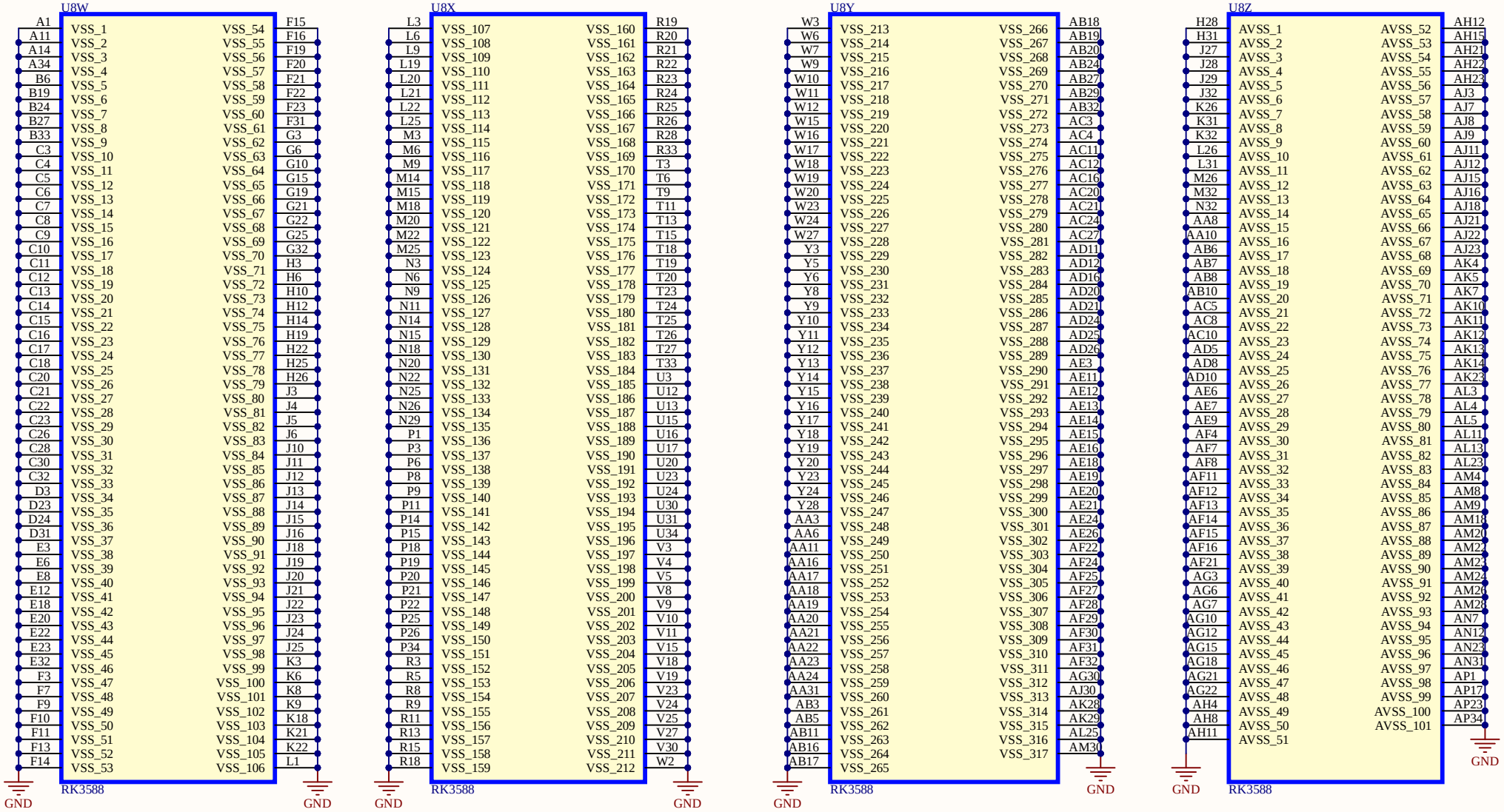



VDD_CPU_BIG0
这个本身就是使能信号
VCC_3V3_S3
R19
100K
R22
120K
BIG/NPU_EN
GND
用于动态调节 CPU 大核心
工作电压的电压选择信号
U3
CPU_BIG0_VSEL
I2C0_SCL_M2
I2C0_SDA_M2
VSEL LX
EN LX
SCL VIN
VOUT VIN
SDA LX
GND LX
GND VIN
AGND VIN
GND GND
GND GND
RK860-2
L11
0.22uH
VCC4V0_SYS
C79
22uf
C81
22uf
Default:0.75V
0.75V≤Vrange≤0.95V
VDD_CPU_BIG0_S0
R20
100R
C71
1uf
C72
22uf
C73
22uf
C74
22uf
C75
22uf
C76
22uf
Feedback from RK3588
VCC_3V3_S0
电子开关，类似于继电器
VCC_3V3_S3
U4
VCC_1V8_S0
R21
1K
C80
0.1uf
VIN VOUT
GND
EN ISET
LPW5209AB5F
R23
3.4K
2A限流
C77
10uf
C78
0.1uf
VDD_CPU_BIG1
U5
CPU_BIG1_VSEL
RK860-3
L12
VDD_CPU_BIG1_S0
FB1
VDD_CPU_BIG1_MEM_S0
120R@100MHz
R24
100R
C82
1uf
C83
22uf
C84
22uf
C85
22uf
C86
22uf
C87
22uf
C88
22uf
C89
22uf
C90
22uf
VDD_NPU
U6
NPU_VSEL
I2C1_SCL_M2
I2C1_SDA_M2
L13
VDD_NPU_S0
R27
100R
C95
1uf
C96
22uf
C97
22uf
C98
22uf
C99
22uf
C100
22uf
C101
22uf
C103
22uf
VCC_1V1_NLDO
VCC4V0_SYS
U7
VIN LX
GND
FB EN
RT8097CHGB
C91
10uf
L14
2.2uH
R26
10K
C102
0.1uf
EXT_PWR_EN
C92
22pf
R25
100K
反馈电压0.6V
R28
120K
VCC_1V1_NLDO_S3
C93
22uf
C94
0.1uf

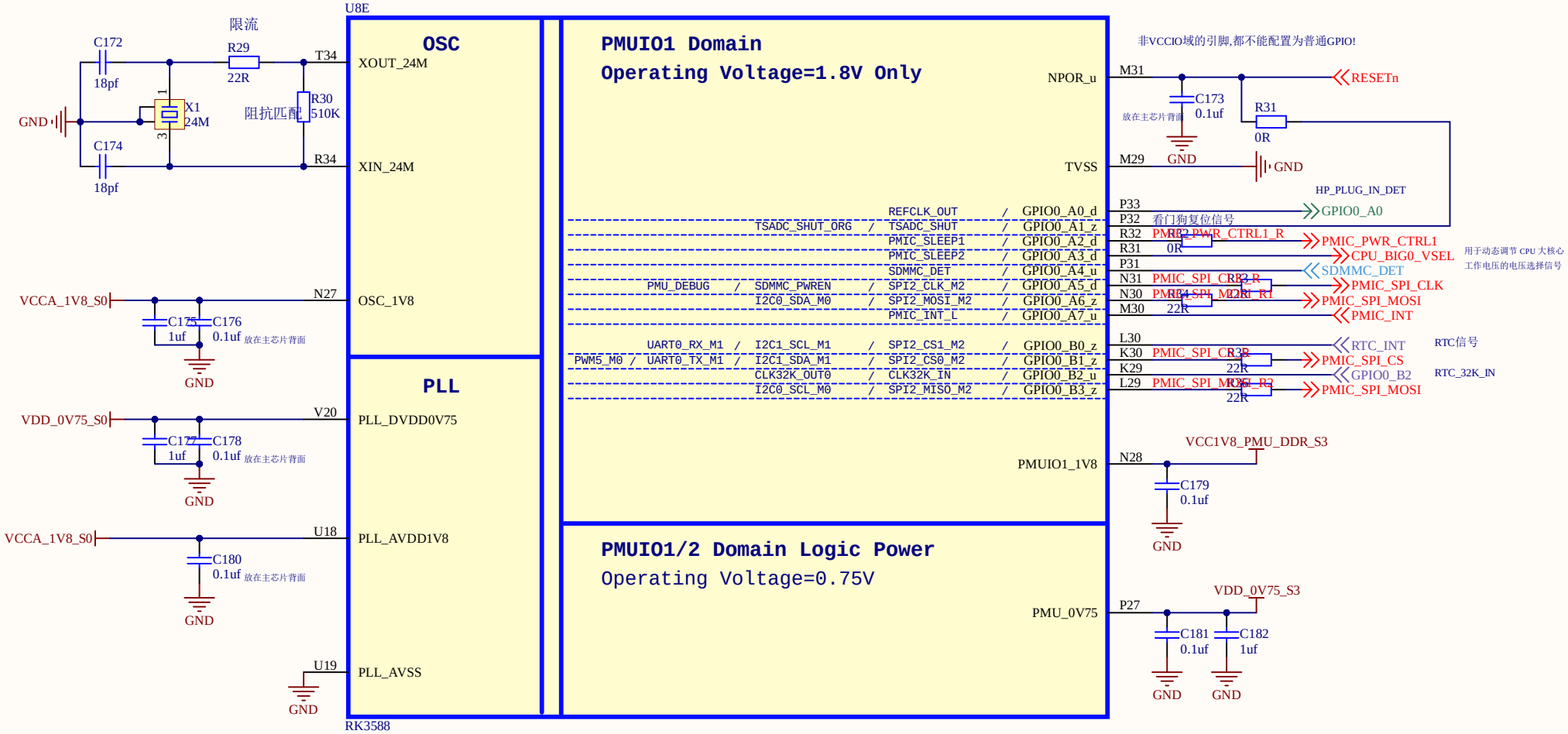
RK3588 POWER



RK3588 GND


U8W
A1 VSS_1 VSS_54 F15
A11 VSS_2 VSS_55 F16
A14 VSS_3 VSS_56 F19
A34 VSS_4 VSS_57 F20
B6 VSS_5 VSS_58 F21
B19 VSS_6 VSS_59 F22
B24 VSS_7 VSS_60 F23
B27 VSS_8 VSS_61 F31
B33 VSS_9 VSS_62 G3
C3 VSS_10 VSS_63 G6
C4 VSS_11 VSS_64 G10
C5 VSS_12 VSS_65 G15
C6 VSS_13 VSS_66 G19
C7 VSS_14 VSS_67 G21
C8 VSS_15 VSS_68 G22
C9 VSS_16 VSS_69 G25
C10 VSS_17 VSS_70 G32
C11 VSS_18 VSS_71 H3
C12 VSS_19 VSS_72 H6
C13 VSS_20 VSS_73 H10
C14 VSS_21 VSS_74 H12
C15 VSS_22 VSS_75 H14
C16 VSS_23 VSS_76 H19
C17 VSS_24 VSS_77 H22
C18 VSS_25 VSS_78 H25
C20 VSS_26 VSS_79 H26
C21 VSS_27 VSS_80 J3
C22 VSS_28 VSS_81 J4
C23 VSS_29 VSS_82 J5
C26 VSS_30 VSS_83 J6
C28 VSS_31 VSS_84 J10
C30 VSS_32 VSS_85 J11
C32 VSS_33 VSS_86 J12
D3 VSS_34 VSS_87 J13
D23 VSS_35 VSS_88 J14
D24 VSS_36 VSS_89 J15
D31 VSS_37 VSS_90 J16
E3 VSS_38 VSS_91 J18
E6 VSS_39 VSS_92 J19
E8 VSS_40 VSS_93 J20
E12 VSS_41 VSS_94 J21
E18 VSS_42 VSS_95 J22
E20 VSS_43 VSS_96 J23
E22 VSS_44 VSS_97 J24
E23 VSS_45 VSS_98 J25
E32 VSS_46 VSS_99 K3
F3 VSS_47 VSS_100 K6
F7 VSS_48 VSS_101 K8
F9 VSS_49 VSS_102 K9
F10 VSS_50 VSS_103 K18
F11 VSS_51 VSS_104 K21
F13 VSS_52 VSS_105 K22
F14 VSS_53 VSS_106 L1
RK3588
GND
GND
U8X
L3 VSS_107 VSS_160 R19
L6 VSS_108 VSS_161 R20
L9 VSS_109 VSS_162 R21
L19 VSS_110 VSS_163 R22
L20 VSS_111 VSS_164 R23
L21 VSS_112 VSS_165 R24
L22 VSS_113 VSS_166 R25
L25 VSS_114 VSS_167 R26
M3 VSS_115 VSS_168 R28
M6 VSS_116 VSS_169 R33
M9 VSS_117 VSS_170 T3
M14 VSS_118 VSS_171 T6
M15 VSS_119 VSS_172 T9
M18 VSS_120 VSS_173 T11
M20 VSS_121 VSS_174 T13
M22 VSS_122 VSS_175 T15
M25 VSS_123 VSS_176 T18
N3 VSS_124 VSS_177 T19
N6 VSS_125 VSS_178 T20
N9 VSS_126 VSS_179 T23
N11 VSS_127 VSS_180 T24
N14 VSS_128 VSS_181 T25
N15 VSS_129 VSS_182 T26
N18 VSS_130 VSS_183 T27
N20 VSS_131 VSS_184 T33
N22 VSS_132 VSS_185 U3
N25 VSS_133 VSS_186 U12
N26 VSS_134 VSS_187 U13
N29 VSS_135 VSS_188 U15
P1 VSS_136 VSS_189 U16
P3 VSS_137 VSS_190 U17
P6 VSS_138 VSS_191 U20
P8 VSS_139 VSS_192 U23
P9 VSS_140 VSS_193 U24
P11 VSS_141 VSS_194 U30
P14 VSS_142 VSS_195 U31
P15 VSS_143 VSS_196 U34
P18 VSS_144 VSS_197 V3
P19 VSS_145 VSS_198 V4
P20 VSS_146 VSS_199 V5
P21 VSS_147 VSS_200 V8
P22 VSS_148 VSS_201 V9
P25 VSS_149 VSS_202 V10
P26 VSS_150 VSS_203 V11
P34 VSS_151 VSS_204 V15
R3 VSS_152 VSS_205 V18
R5 VSS_153 VSS_206 V19
R8 VSS_154 VSS_207 V23
R9 VSS_155 VSS_208 V24
R11 VSS_156 VSS_209 V25
R13 VSS_157 VSS_210 V27
R15 VSS_158 VSS_211 V30
R18 VSS_159 VSS_212 W2
RK3588
GND
GND
U8Y
W3 VSS_213 VSS_266 AB18
W6 VSS_214 VSS_267 AB19
W7 VSS_215 VSS_268 AB20
W9 VSS_216 VSS_269 AB24
W10 VSS_217 VSS_270 AB27
W11 VSS_218 VSS_271 AB29
W12 VSS_219 VSS_272 AB32
W15 VSS_220 VSS_273 AC3
W16 VSS_221 VSS_274 AC4
W17 VSS_222 VSS_275 AC11
W18 VSS_223 VSS_276 AC12
W19 VSS_224 VSS_277 AC16
W20 VSS_225 VSS_278 AC20
W23 VSS_226 VSS_279 AC21
W24 VSS_227 VSS_280 AC24
W27 VSS_228 VSS_281 AC27
Y3 VSS_229 VSS_282 AD11
Y5 VSS_230 VSS_283 AD12
Y6 VSS_231 VSS_284 AD16
Y8 VSS_232 VSS_285 AD20
Y9 VSS_233 VSS_286 AD21
Y10 VSS_234 VSS_287 AD24
Y11 VSS_235 VSS_288 AD25
Y12 VSS_236 VSS_289 AD26
Y13 VSS_237 VSS_290 AE3
Y14 VSS_238 VSS_291 AE11
Y15 VSS_239 VSS_292 AE12
Y16 VSS_240 VSS_293 AE13
Y17 VSS_241 VSS_294 AE14
Y18 VSS_242 VSS_295 AE15
Y19 VSS_243 VSS_296 AE16
Y20 VSS_244 VSS_297 AE18
Y23 VSS_245 VSS_298 AE19
Y24 VSS_246 VSS_299 AE20
Y28 VSS_247 VSS_300 AE21
AA3 VSS_248 VSS_301 AE24
AA6 VSS_249 VSS_302 AE26
AA11 VSS_250 VSS_303 AF22
AA16 VSS_251 VSS_304 AF24
AA17 VSS_252 VSS_305 AF25
AA18 VSS_253 VSS_306 AF27
AA19 VSS_254 VSS_307 AF28
AA20 VSS_255 VSS_308 AF29
AA21 VSS_256 VSS_309 AF30
AA22 VSS_257 VSS_310 AF31
AA23 VSS_258 VSS_311 AF32
AA24 VSS_259 VSS_312 AG30
AA31 VSS_260 VSS_313 AJ30
AB3 VSS_261 VSS_314 AK28
AB5 VSS_262 VSS_315 AK29
AB11 VSS_263 VSS_316 AL25
AB16 VSS_264 VSS_317 AM30
AB17 VSS_265
RK3588
GND
GND
U8Z
H28 AVSS_1 AVSS_52 AH12
H31 AVSS_2 AVSS_53 AH15
J27 AVSS_3 AVSS_54 AH21
J28 AVSS_4 AVSS_55 AH22
J29 AVSS_5 AVSS_56 AH23
J32 AVSS_6 AVSS_57 AJ3
K26 AVSS_7 AVSS_58 AJ7
K31 AVSS_8 AVSS_59 AJ8
K32 AVSS_9 AVSS_60 AJ9
L26 AVSS_10 AVSS_61 AJ11
L31 AVSS_11 AVSS_62 AJ12
M26 AVSS_12 AVSS_63 AJ15
M32 AVSS_13 AVSS_64 AJ16
N32 AVSS_14 AVSS_65 AJ18
AA8 AVSS_15 AVSS_66 AJ21
AA10 AVSS_16 AVSS_67 AJ22
AB6 AVSS_17 AVSS_68 AJ23
AB7 AVSS_18 AVSS_69 AK4
AB8 AVSS_19 AVSS_70 AK5
AB10 AVSS_20 AVSS_71 AK7
AC5 AVSS_21 AVSS_72 AK10
AC8 AVSS_22 AVSS_73 AK11
AC10 AVSS_23 AVSS_74 AK12
AD5 AVSS_24 AVSS_75 AK13
AD8 AVSS_25 AVSS_76 AK14
AD10 AVSS_26 AVSS_77 AK23
AE6 AVSS_27 AVSS_78 AL3
AE7 AVSS_28 AVSS_79 AL4
AE9 AVSS_29 AVSS_80 AL5
AF4 AVSS_30 AVSS_81 AL11
AF7 AVSS_31 AVSS_82 AL13
AF8 AVSS_32 AVSS_83 AL23
AF11 AVSS_33 AVSS_84 AM4
AF12 AVSS_34 AVSS_85 AM8
AF13 AVSS_35 AVSS_86 AM9
AF14 AVSS_36 AVSS_87 AM18
AF15 AVSS_37 AVSS_88 AM20
AF16 AVSS_38 AVSS_89 AM22
AF21 AVSS_39 AVSS_90 AM23
AG3 AVSS_40 AVSS_91 AM24
AG6 AVSS_41 AVSS_92 AM26
AG7 AVSS_42 AVSS_93 AM28
AG10 AVSS_43 AVSS_94 AN7
AG12 AVSS_44 AVSS_95 AN12
AG15 AVSS_45 AVSS_96 AN23
AG18 AVSS_46 AVSS_97 AN31
AG21 AVSS_47 AVSS_98 AP1
AG22 AVSS_48 AVSS_99 AP17
AH4 AVSS_49 AVSS_100 AP23
AH8 AVSS_50 AVSS_101 AP34
AH11 AVSS_51
GND
GND
RK3588

RK3588 OSC/PLL/PMUIO1



RK3588 PMUIO2

电源管理、系统复位、基本初始化和安全启动相关

U8F

PMUIO2 Domain

Operating Voltage=1.8V/3.3V

	UART2_TX_M0			I2S1_MCLK_M1	PCIE30X1_1_CLKREQN_M0		I2C1_SCL_M0	JTAG_TCK_M2		GPIO0_B5_d
	UART2_RX_M0			I2S1_SCLK_M1	PCIE30X1_1_WAKEN_M0		I2C1_SDA_M0	JTAG_TMS_M2		GPIO0_B6_d
		CAN0_TX_M0		I2S1_LRCK_M1	PCIE30X1_1_PERSTN_M0	SPI0_CS1_M0	I2C2_SCL_M0	PWM0_M0		GPIO0_B7_d
		CAN0_RX_M0	PDM0_CLK0_M1		PCIE30X1_0_CLKREQN_M0	SPI0_MOSI_M0	I2C2_SDA_M0	PWM1_M0		GPIO0_C0_d
								PMIC_SLEEP3		GPIO0_C1_d
								PMIC_SLEEP4		GPIO0_C2_d
								PMIC_SLEEP5		GPIO0_C3_d
	UART0_RX_M0	DP0_HPDIN_M1	PDM0_CLK1_M1		PCIE30X1_0_WAKEN_M0		I2C4_SDA_M2	PWM2_M0		GPIO0_C4_d
PWM4_M0	UART0_TX_M0	DP1_HPDIN_M1		I2S1_SDI0_M1	PCIE30X1_0_PERSTN_M0		I2C4_SCL_M2	GPU_AVS		GPIO0_C5_u
PWM5_M1	UART0_RTSN	SATA_CP_POD		I2S1_SDI1_M1	PCIE30X4_CLKREQN_M0	SPI0_CLK_M0		NPU_AVS		GPIO0_C6_u
	UART1_RTSN_M2		PDM0_SDI0_M1	I2S1_SDI2_M1	PCIE30X4_WAKEN_M0	SPI0_MISO_M0	I2C6_SDA_M0	PWM6_M0		GPIO0_C7_d
	UART1_CTSN_M2		PDM0_SDI1_M1	I2S1_SDI3_M1	PCIE30X4_PERSTN_M0	SPI3_MISO_M2	I2C6_SCL_M0	PWM7_IR_M0		GPIO0_D0_d
HDMI_TX0_CEC_M1	UART1_TX_M2	UART0_CTSN	HDMI_RX_SDA_M0	I2S1_SDO0_M1	PCIE30X2_CLKREQN_M0	SPI0_CS0_M0	I2C0_SCL_M2	CPU_BIG0_AVS		GPIO0_D1_u
HDMI_TX1_CEC_M1	UART1_RX_M2		HDMI_RX_SCL_M0	I2S1_SDO1_M1	PCIE30X2_WAKEN_M0	SPI3_MOSI_M2	I2C0_SDA_M2			GPIO0_D2_u
						SPI3_CLK_M2		LITCPU_AVS		GPIO0_D3_u
HDMI_TX0_SDA_M1	SATA_CPDET	CAN2_RX_M1	PDM0_SDI2_M1	I2S1_SDO2_M1	PCIE30X2_PERSTN_M0	SPI3_CS0_M2	I2C1_SCL_M2	PWM3_IR_M0		GPIO0_D4_u
HDMI_TX0_SCL_M1	SATA_MP_SWITCH	CAN2_TX_M1		I2S1_SDO3_M1		SPI3_CS1_M2	I2C1_SDA_M2	CPU_BIG1_AVS		GPIO0_D5_u
			PDM0_SDI3_M1					PMIC_SLEEP6		GPIO0_D6_d
									PMUIO2_1V8	
									PMUIO2	

RK3588

需要串接100ohm电阻并加上tvs管

P29	UART2_TX_M0_DEBUG		调试串口
R29	UART2_RX_M0_DEBUG		调试串口
T28	GPIO0_B7		M2EKEY_PWR_EN
T31	PCIE30X1_0_CLKREQN_M0		底板M2 E KEY控制信号
U32	NPU_VSEL		
T32	PMIC_PWR_CTRL3_R	R37 100K	PMIC_PWR_CTRL3
T30	PMIC_PWR_CTRL2_R	R38 100K	PMIC_PWR_CTRL2
R30	PCIE30X1_0_WAKEN_M0		底板M2 E KEY控制信号
P30	PCIE30X1_0_PERSTN_M0		底板M2 E KEY控制信号
T29	GPIO0_C6		M2EKEY_nWDISABLE
V31	GPIO0_C7		EARPHONE_CTL
W31			
W30	I2C0_SCL_M2		底板RTC芯片 IO扩展芯片和CAM0
W29	I2C0_SDA_M2		底板RTC芯片 IO扩展芯片和CAM0
U33	GPIO0_D3		底板typec芯片 FUSB302_INT
V29	I2C1_SCL_M2		底板typec芯片
V28	I2C1_SDA_M2		底板typec芯片
W28	CPU_BIG1_VSEL		

R27 — VCC1V8_PMU_DDR_S3

C183 0.1uf — 放在主芯片背面 — GND

P28 — VCC_3V3_S3

C184 0.1uf — 放在主芯片背面 — GND

I2C1_SDA_M2 — R39 2.2K — VCC_3V3_S3

I2C1_SCL_M2 — R41 2.2K — VCC_3V3_S3

PMIC_PWR_CTRL3 — R40 20K — GND

PMIC_PWR_CTRL2 — R42 20K — GND

I2C0_SDA_M2 — R43 2.2K — VCC_3V3_S3

I2C0_SCL_M2 — R44 2.2K — VCC_3V3_S3

RK3588 DDR Controler CH0

DDR控制器接口

U8A

DDR_CH0_DQ0_A	U1	DDR_CH0_DQ0_A	DDR_CH0_DQ0_B	H1	DDR_CH0_DQ0_B
DDR_CH0_DQ1_A	T2	DDR_CH0_DQ1_A	DDR_CH0_DQ1_B	J2	DDR_CH0_DQ1_B
DDR_CH0_DQ2_A	T1	DDR_CH0_DQ2_A	DDR_CH0_DQ2_B	J1	DDR_CH0_DQ2_B
DDR_CH0_DQ3_A	R2	DDR_CH0_DQ3_A	DDR_CH0_DQ3_B	K2	DDR_CH0_DQ3_B
DDR_CH0_DQ4_A	W1	DDR_CH0_DQ4_A	DDR_CH0_DQ4_B	F1	DDR_CH0_DQ4_B
DDR_CH0_DQ5_A	V2	DDR_CH0_DQ5_A	DDR_CH0_DQ5_B	G2	DDR_CH0_DQ5_B
DDR_CH0_DQ6_A	V1	DDR_CH0_DQ6_A	DDR_CH0_DQ6_B	G1	DDR_CH0_DQ6_B
DDR_CH0_DQ7_A	U2	DDR_CH0_DQ7_A	DDR_CH0_DQ7_B	H2	DDR_CH0_DQ7_B
DDR_CH0_DQ8_A	AB2	DDR_CH0_DQ8_A	DDR_CH0_DQ8_B	D2	DDR_CH0_DQ8_B
DDR_CH0_DQ9_A	AB1	DDR_CH0_DQ9_A	DDR_CH0_DQ9_B	C1	DDR_CH0_DQ9_B
DDR_CH0_DQ10_A	AC1	DDR_CH0_DQ10_A	DDR_CH0_DQ10_B	C2	DDR_CH0_DQ10_B
DDR_CH0_DQ11_A	AC2	DDR_CH0_DQ11_A	DDR_CH0_DQ11_B	B1	DDR_CH0_DQ11_B
DDR_CH0_DQ12_A	Y1	DDR_CH0_DQ12_A	DDR_CH0_DQ12_B	F2	DDR_CH0_DQ12_B
DDR_CH0_DQ13_A	Y2	DDR_CH0_DQ13_A	DDR_CH0_DQ13_B	E1	DDR_CH0_DQ13_B
DDR_CH0_DQ14_A	AA1	DDR_CH0_DQ14_A	DDR_CH0_DQ14_B	E2	DDR_CH0_DQ14_B
DDR_CH0_DQ15_A	AA2	DDR_CH0_DQ15_A	DDR_CH0_DQ15_B	D1	DDR_CH0_DQ15_B
					数据传输主体
DDR_CH0_DM0_A	Y4	DDR_CH0_DM0_A	DDR_CH0_DM0_B	G4	DDR_CH0_DM0_B
DDR_CH0_DM1_A	AB4	DDR_CH0_DM1_A	DDR_CH0_DM1_B	E4	DDR_CH0_DM1_B
					写数据掩码
DDR_CH0_DQS0P_A	U5	DDR_CH0_DQS0P_A	DDR_CH0_DQS0P_B	J8	DDR_CH0_DQS0P_B
DDR_CH0_DQS0N_A	U4	DDR_CH0_DQS0N_A	DDR_CH0_DQS0N_B	J7	DDR_CH0_DQS0N_B
DDR_CH0_DQS1P_A	AA5	DDR_CH0_DQS1P_A	DDR_CH0_DQS1P_B	F5	DDR_CH0_DQS1P_B
DDR_CH0_DQS1N_A	AA4	DDR_CH0_DQS1N_A	DDR_CH0_DQS1N_B	F4	DDR_CH0_DQS1N_B
					数据选通
	V7	DDR_CH0_WCK0P_A	DDR_CH0_WCK0P_B	K5	
	V6	DDR_CH0_WCK0N_A	DDR_CH0_WCK0N_B	K4	
	W4	DDR_CH0_WCK1P_A	DDR_CH0_WCK1P_B	H4	
	W5	DDR_CH0_WCK1N_A	DDR_CH0_WCK1N_B	H5	
DDR_CH0_A0_A	T7	DDR_CH0_A0_A	DDR_CH0_A0_B	M8	DDR_CH0_A0_B
DDR_CH0_A1_A	T8	DDR_CH0_A1_A	DDR_CH0_A1_B	M5	DDR_CH0_A1_B
DDR_CH0_A2_A	P4	DDR_CH0_A2_A	DDR_CH0_A2_B	N5	DDR_CH0_A2_B
DDR_CH0_A3_A	P5	DDR_CH0_A3_A	DDR_CH0_A3_B	N4	DDR_CH0_A3_B
DDR_CH0_A4_A	R1	DDR_CH0_A4_A	DDR_CH0_A4_B	K1	DDR_CH0_A4_B
DDR_CH0_A5_A	P2	DDR_CH0_A5_A	DDR_CH0_A5_B	L2	DDR_CH0_A5_B
	T5	DDR_CH0_A6_A	DDR_CH0_A6_B	M7	
					地址/命令总线
DDR_CH0_CLKP_A	N2	DDR_CH0_CK_A	DDR_CH0_CK_B	M2	DDR_CH0_CLKP_B
DDR_CH0_CLKN_A	N1	DDR_CH0_CKB_A	DDR_CH0_CKB_B	M1	DDR_CH0_CLKN_B
					差分系统时钟
DDR_CH0_LP4/4X_CKE0_A	P7	DDR_CH0_LP4/4X_CKE0/LP5_CS0_A	DDR_CH0_LP4/4X_CKE0/LP5_CS0_B	L5	DDR_CH0_LP4/4X_CKE0_B
DDR_CH0_LP4/4X_CKE1_A	N7	DDR_CH0_LP4/4X_CKE1/LP5_CS1_A	DDR_CH0_LP4/4X_CKE1/LP5_CS1_B	L4	DDR_CH0_LP4/4X_CKE1_B
					时钟使能
DDR_CH0_LP4/4X_CS0_A	R6	DDR_CH0_LP4/4X_CS0_A	DDR_CH0_LP4/4X_CS0_B	L7	DDR_CH0_LP4/4X_CS0_B
DDR_CH0_LP4/4X_CS1_A	R7	DDR_CH0_LP4/4X_CS1_A	DDR_CH0_LP4/4X_CS1_B	L8	DDR_CH0_LP4/4X_CS1_B
					片选
DDR_RESET	T4	DDR_CH0_RESET_A	DDR_CH0_RESET_B	K7	
VDDQ_DDR_S0 — R45 240R	W8	DDR_CH0_ZQ_A	DDR_CH0_ZQ_B	H7	R46 240R — VDDQ_DDR_S0

DDR_PLL POWER

VDDA_DDR_PLL_S0	N12	DDR_CH0_PLL_DVDD 0.75V-0.85V
AVDD1V8_DDR_PLL_S0	M12	DDR_CH0_PLL_AVDD1V8 1.8V
GND	M11	DDR_CH0_PLL_AVSS

LP4/4X_CKE&LP5_CS & Reset Power

LPDDR4/4X=1.1V
LPDDR5=1.05V

DDR_CH0_VDDQ_CKE — N8 — VDDQ_DDR_CKE_S3 控制信号的I/O缓冲器电源

3.VDDQ_LP4/4X_CKE/LP5_CS: power for LP4_CKE/LP5_CS and RESET, lpddr4X=1.1V/lpddr5=1.05V
VDDQ_LP4/4X_CKE: 为LPDDR4/4X的CKE信号供电，LPDDR4X电压为1.1V

MEMORY INTERFACE POWER

N13	DDR_CH0_VDD_MIF_0	0.75V-0.85V
P13	DDR_CH0_VDD_MIF_1	

CK Power

LPDDR4/4X=0.6V
LPDDR5=0.5V

DDR_CH0_VDDQ_CK — L10 — VDDQ_DDR_CK_S0 系统时钟的I/O缓冲器电源

1.Hold power of CLK during retention times.
在保持阶段期间，为CLK（时钟）保持供电
4.VDDQ_CK: power for CK, LPDDR4/4X=0.6V/LPDDR5=0.5V
VDDQ_CK: 为CK（时钟）供电，LPDDR4/4X电压为0.6V

核心逻辑电源 VDD_DDR_S0
2.Sequence:VDD-VDDQ_CKE-VDDQ
上电顺序: VDDQ_DDR_S0 VDDQ_DDR_CKE_S3 VDDQ_DDR_S0

DIGITAL CORE POWER

U11	DDR_CH0_VDD_0	0.75V-0.85V
T12	DDR_CH0_VDD_1	
R12	DDR_CH0_VDD_2	
P12	DDR_CH0_VDD_3	

DDR IO POWER

(Except for ck, cke and reset)

LPDDR4/4X=0.6V
LPDDR5=0.5V

DDR_CH0_VDDQ_0	M10	VDDQ_DDR_S0
DDR_CH0_VDDQ_1	N10	
DDR_CH0_VDDQ_2	P10	
DDR_CH0_VDDQ_3	R10	
DDR_CH0_VDDQ_4	T10	

数据接口电源
VDDQ: Power for DDR IO (except for ck, cke and reset); LPDDR4/4X=0.6V/LPDDR5=0.5V
DDQ：为DDR的输入/输出接口供电（除CK、CKE和RESET外）；LPDDR4/4X电压为0.6V

RK3588

RK3588 DDR Controler CH1

DDR控制器接口

U8B

DDR_CH1_DQ0_C	A8	DDR_CH1_DQ0_C	DDR_CH1_DQ0_D	A17	DDR_CH1_DQ0_D
DDR_CH1_DQ1_C	B9	DDR_CH1_DQ1_C	DDR_CH1_DQ1_D	B16	DDR_CH1_DQ1_D
DDR_CH1_DQ2_C	A9	DDR_CH1_DQ2_C	DDR_CH1_DQ2_D	A16	DDR_CH1_DQ2_D
DDR_CH1_DQ3_C	B10	DDR_CH1_DQ3_C	DDR_CH1_DQ3_D	B15	DDR_CH1_DQ3_D
DDR_CH1_DQ4_C	A6	DDR_CH1_DQ4_C	DDR_CH1_DQ4_D	A19	DDR_CH1_DQ4_D
DDR_CH1_DQ5_C	B7	DDR_CH1_DQ5_C	DDR_CH1_DQ5_D	B18	DDR_CH1_DQ5_D
DDR_CH1_DQ6_C	A7	DDR_CH1_DQ6_C	DDR_CH1_DQ6_D	A18	DDR_CH1_DQ6_D
DDR_CH1_DQ7_C	B8	DDR_CH1_DQ7_C	DDR_CH1_DQ7_D	B17	DDR_CH1_DQ7_D
DDR_CH1_DQ8_C	A3	DDR_CH1_DQ8_C	DDR_CH1_DQ8_D	A22	DDR_CH1_DQ8_D
DDR_CH1_DQ9_C	B3	DDR_CH1_DQ9_C	DDR_CH1_DQ9_D	B22	DDR_CH1_DQ9_D
DDR_CH1_DQ10_C	A2	DDR_CH1_DQ10_C	DDR_CH1_DQ10_D	A23	DDR_CH1_DQ10_D
DDR_CH1_DQ11_C	B2	DDR_CH1_DQ11_C	DDR_CH1_DQ11_D	B23	DDR_CH1_DQ11_D
DDR_CH1_DQ12_C	A5	DDR_CH1_DQ12_C	DDR_CH1_DQ12_D	A20	DDR_CH1_DQ12_D
DDR_CH1_DQ13_C	B5	DDR_CH1_DQ13_C	DDR_CH1_DQ13_D	B20	DDR_CH1_DQ13_D
DDR_CH1_DQ14_C	A4	DDR_CH1_DQ14_C	DDR_CH1_DQ14_D	A21	DDR_CH1_DQ14_D
DDR_CH1_DQ15_C	B4	DDR_CH1_DQ15_C	DDR_CH1_DQ15_D	B21	DDR_CH1_DQ15_D
					数据传输主体
DDR_CH1_DM0_C	F8	DDR_CH1_DM0_C	DDR_CH1_DM0_D	D20	DDR_CH1_DM0_D
DDR_CH1_DM1_C	D4	DDR_CH1_DM1_C	DDR_CH1_DM1_D	D22	DDR_CH1_DM1_D
					写数据掩码
DDR_CH1_DQS0P_C	E9	DDR_CH1_DQS0P_C	DDR_CH1_DQS0P_D	H16	DDR_CH1_DQS0P_D
DDR_CH1_DQS0N_C	D9	DDR_CH1_DQS0N_C	DDR_CH1_DQS0N_D	G16	DDR_CH1_DQS0N_D
DDR_CH1_DQS1P_C	E5	DDR_CH1_DQS1P_C	DDR_CH1_DQS1P_D	D21	DDR_CH1_DQS1P_D
DDR_CH1_DQS1N_C	D5	DDR_CH1_DQS1N_C	DDR_CH1_DQS1N_D	E21	DDR_CH1_DQS1N_D
					数据选通
	G9	DDR_CH1_WCK0P_C	DDR_CH1_WCK0P_D	E17	
	H9	DDR_CH1_WCK0N_C	DDR_CH1_WCK0N_D	D17	
	D7	DDR_CH1_WCK1P_C	DDR_CH1_WCK1P_D	H18	
	E7	DDR_CH1_WCK1N_C	DDR_CH1_WCK1N_D	G18	
DDR_CH1_A0_C	G12	DDR_CH1_A0_C	DDR_CH1_A0_D	H15	DDR_CH1_A0_D
DDR_CH1_A1_C	F12	DDR_CH1_A1_C	DDR_CH1_A1_D	G14	DDR_CH1_A1_D
DDR_CH1_A2_C	E13	DDR_CH1_A2_C	DDR_CH1_A2_D	G13	DDR_CH1_A2_D
DDR_CH1_A3_C	D13	DDR_CH1_A3_C	DDR_CH1_A3_D	E14	DDR_CH1_A3_D
DDR_CH1_A4_C	A10	DDR_CH1_A4_C	DDR_CH1_A4_D	A15	DDR_CH1_A4_D
DDR_CH1_A5_C	B11	DDR_CH1_A5_C	DDR_CH1_A5_D	B14	DDR_CH1_A5_D
	D10	DDR_CH1_A6_C	DDR_CH1_A6_D	D14	
					地址/命令总线
DDR_CH1_CLKP_C	B12	DDR_CH1_CK_C	DDR_CH1_CK_D	B13	DDR_CH1_CLKP_D
DDR_CH1_CLKN_C	A12	DDR_CH1_CKB_C	DDR_CH1_CKB_D	A13	DDR_CH1_CLKN_D
					差分系统时钟
DDR_CH1_LP4/4X_CKE0_C	D11	DDR_CH1_LP4/4X_CKE0/LP5_CS0_C	DDR_CH1_LP4/4X_CKE0/LP5_CS0_D	D16	DDR_CH1_LP4/4X_CKE0_D
DDR_CH1_LP4/4X_CKE1_C	E11	DDR_CH1_LP4/4X_CKE1/LP5_CS1_C	DDR_CH1_LP4/4X_CKE1/LP5_CS1_D	E16	DDR_CH1_LP4/4X_CKE1_D
					时钟使能
DDR_CH1_LP4/4X_CS0_C	G11	DDR_CH1_LP4/4X_CS0_C	DDR_CH1_LP4/4X_CS0_D	E19	DDR_CH1_LP4/4X_CS0_D
DDR_CH1_LP4/4X_CS1_C	H11	DDR_CH1_LP4/4X_CS1_C	DDR_CH1_LP4/4X_CS1_D	D19	DDR_CH1_LP4/4X_CS1_D
					片选
	E10	DDR_CH1_RESET_C	DDR_CH1_RESET_D	C19	
VDDQ_DDR_S0 — R47 240R	G8	DDR_CH1_ZQ_C	DDR_CH1_ZQ_D	F18	R48 240R — VDDQ_DDR_S0

DDR_PLL POWER

VDDA_DDR_PLL_S0	L15	DDR_CH1_PLL_DVDD 0.75V-0.85V
AVDD1V8_DDR_PLL_S0	K16	DDR_CH1_PLL_AVDD1V8 1.8V
GND	L16	DDR_CH1_PLL_AVSS

LP4/4X_CKE&LP5_CS & Reset Power

LPDDR4/4X=1.1V
LPDDR5=1.05V

DDR_CH1_VDDQ_CKE — H13 — VDDQ_DDR_CKE_S3 控制信号的I/O缓冲器电源

MEMORY INTERFACE POWER

L17	DDR_CH1_VDD_MIF_0	0.75V-0.85V
L18	DDR_CH1_VDD_MIF_1	

CK Power

LPDDR4/4X=0.6V
LPDDR5=0.5V

DDR_CH1_VDDQ_CK — M13 — VDDQ_DDR_CK_S0 系统时钟的I/O缓冲器电源

VDD_DDR_S0

DIGITAL CORE POWER

L11	DDR_CH1_VDD_0	0.75V-0.85V
L12	DDR_CH1_VDD_1	
L13	DDR_CH1_VDD_2	
L14	DDR_CH1_VDD_3	

DDR IO POWER

(Except for ck, cke and reset)

LPDDR4/4X=0.6V
LPDDR5=0.5V

DDR_CH1_VDDQ_0	K11	VDDQ_DDR_S0
DDR_CH1_VDDQ_1	K12	
DDR_CH1_VDDQ_2	K13	
DDR_CH1_VDDQ_3	K14	
DDR_CH1_VDDQ_4	K15	

RK3588

DDR Filter

RK3588和DDR内存颗粒的I/O接口 VDD2_DDR_S3 ---------> 控制信号的I/O缓冲器电源 VDDQ_DDR_CKE_S3

DDR相关的辅助电路供电 VDDQ_DDR_S0 ---------> 系统时钟的I/O缓冲器电源 VDDQ_DDR_CK_S0

VDDQ_DDR_S0: C193 10uf, C194 1uf, C195 1uf, C196 0.1uf, C197 0.1uf, C198 0.1uf — GND
VDDQ_DDR_CK_S0: C199 1uf — GND
VDDQ_DDR_CKE_S3: C200 1uf — GND

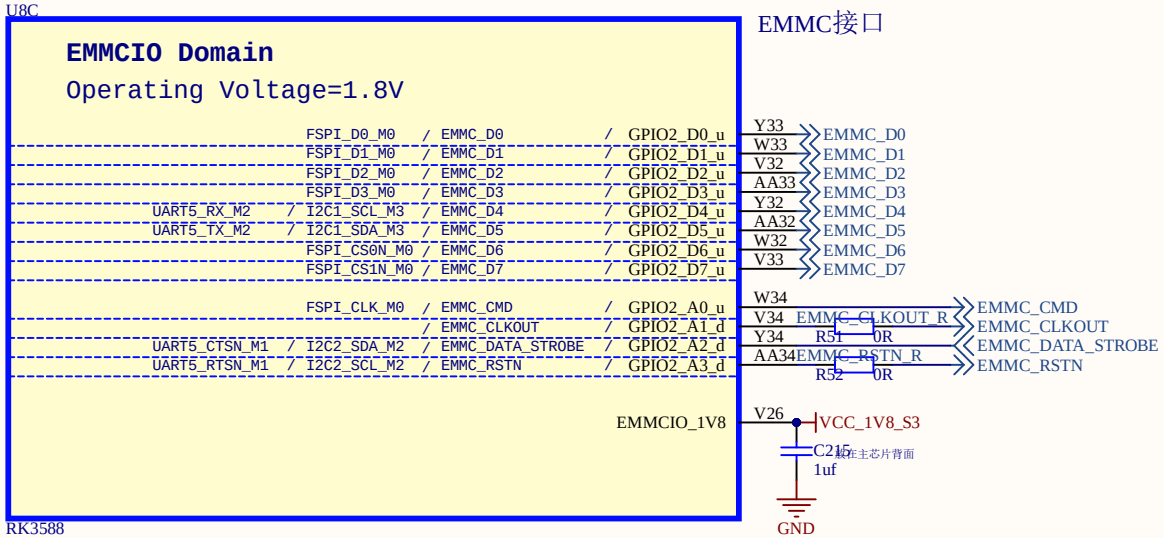
VDD_DDR_S0: C208 10uf, C209 4.7uf, C210 0.1uf — GND
AVDD1V8_DDR_PLL_S0: C211 1uf — GND
VDDA_DDR_PLL_S0: C212 1uf — GND
VDD_DDR_S0: C213 1uf, C214 0.1uf — GND

DDR Filter

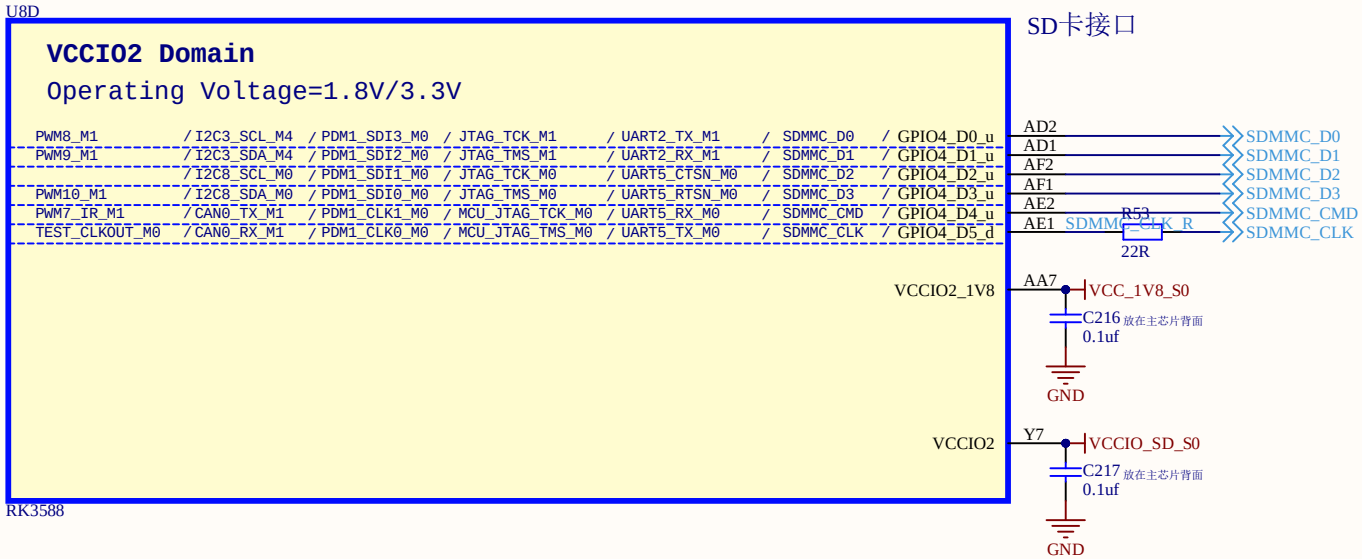
VDDQ_DDR_S0: C185 10uf, C186 1uf, C187 1uf, C188 0.1uf, C189 0.1uf, C190 0.1uf — GND
VDDQ_DDR_CK_S0: C191 1uf — GND
VDDQ_DDR_CKE_S3: C192 1uf — GND

VDD_DDR_S0: C201 10uf, C202 4.7uf, C203 0.1uf — GND
AVDD1V8_DDR_PLL_S0: C204 1uf — GND
VDDA_DDR_PLL_S0: C205 1uf — GND
VDD_DDR_S0: C206 1uf, C207 0.1uf — GND

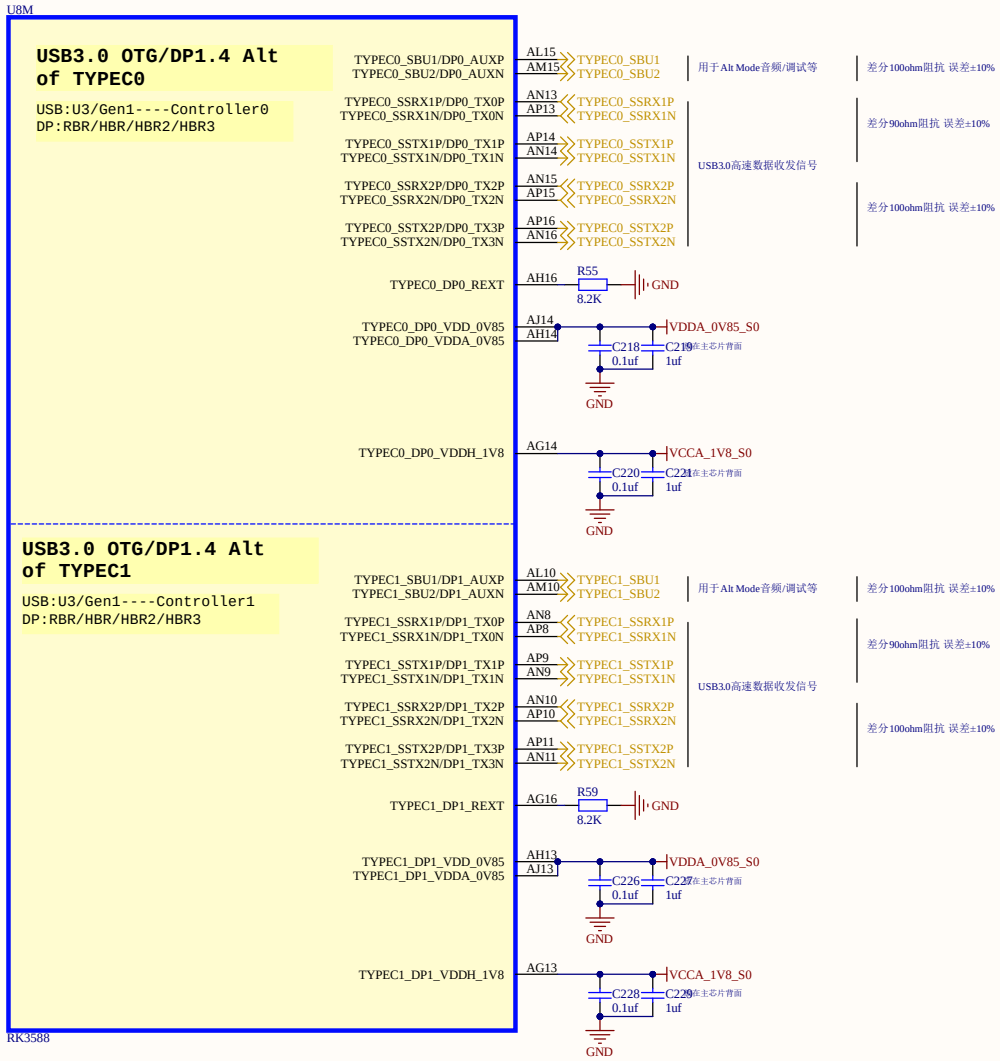
RK3588 EMMCIO Domain



RK3588 VCCIO2 Domain



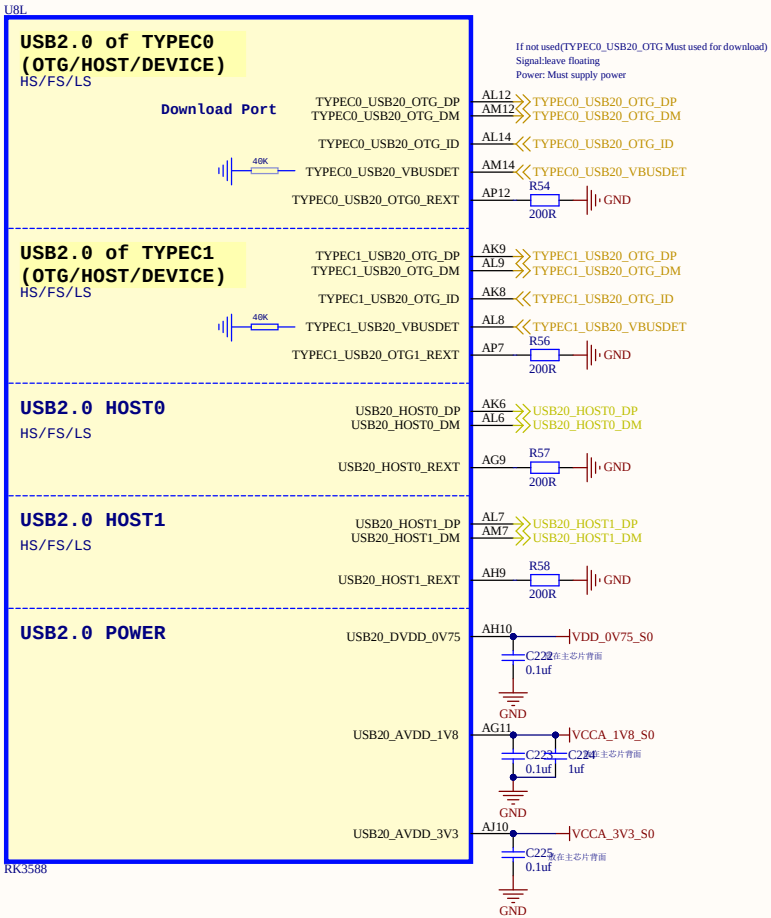
RK3588 TYPEC/DP



USB30/DP1.4 Alt Mode Configuration

Option1	DP x4Lane	DP_TX_Lane0-3
Option2	USB30 x4Lane	DP_TX_Lane0-3
Option3	USB30X2Lane+DPX2Lane	USB30:Lane0 Lane1 DP:Lane2 Lane3
Option4	USB30X2Lane+DPX2Lane	USB30:Lane2 Lane3 DP:Lane0 Lane1

RK3588 USB2.0 HOST/OTG



The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V

USB20_VBUSDET引脚内部有一个40K欧姆的下拉电阻接地。
该电阻与外部串联的30K欧姆电阻共同作用形成一个电压。 VBUSDET引脚电压范围≤3.3V

RK3588 VCCIO1

U8G

VCCIO1 Domain

Operating Voltage=1.8V

SPI4_MISO_M0	UART3_RX_M0		I2C3_SDA_M0				GPIO1_C0_z
SPI4_MOSI_M0	UART3_TX_M0		I2C3_SCL_M0				GPIO1_C1_z
SPI4_CLK_M0	UART3_RTSN	PWM3_IR_M2	I2C6_SDA_M1		I2S0_MCLK		GPIO1_C2_d
SPI4_CS0_M0	UART3_CTSN	PWM7_IR_M2	I2C6_SCL_M1		I2S0_SCLK		GPIO1_C3_d
SPI4_CS1_M0		PWM11_IR_M2	I2C2_SDA_M3	PDM0_CLK1_M0			GPIO1_C4_d
	UART4_RTSN		I2C2_SCL_M3		I2S0_LRCK		GPIO1_C5_d
		PWM15_IR_M2	I2C4_SDA_M4	PDM0_CLK0_M0			GPIO1_C6_d
	UART4_CTSN		I2C4_SCL_M4		I2S0_SDO0		GPIO1_C7_d
SPI1_MISO_M2	UART6_TX_M2		I2C7_SCL_M0		I2S0_SDO1		GPIO1_D0_d
SPI1_MOSI_M2	UART6_RX_M2		I2C7_SDA_M0	PDM0_SDI1_M0	I2S0_SDO2/I2S0_SDI3		GPIO1_D1_d
SPI1_CLK_M2	UART4_TX_M0	PWM0_M1	I2C1_SCL_M4	PDM0_SDI2_M0	I2S0_SDO3/I2S0_SDI2		GPIO1_D2_d
SPI1_CS0_M2	UART4_RX_M0	PWM1_M1	I2C1_SDA_M4	PDM0_SDI3_M0	I2S0_SDI1		GPIO1_D3_d
					I2S0_SDI0		GPIO1_D4_d
SPI1_CS1_M2				PDM0_SDI0_M0			GPIO1_D5_d

VCCIO1_1V8

RK3588

G29	GPIO1_C0	LCD0_PWR_EN
G27	GPIO1_C1	连接底板排针
F30	I2S0_MCLK	底板音频编解码控制
E31	I2S0_SCLK	底板音频编解码控制
E30	GPIO1_C4	FAN_CTRL
D30	I2S0_LRCK	底板音频编解码控制
D29	GPIO1_C6	SYS_LED
E29	I2S0_SDO0	底板音频编解码控制
F26	I2C7_SCL_M0	底板音频编解码控制
F27	I2C7_SDA_M0	底板音频编解码控制
F28		
E28	GPIO1_D3	SATA_PWR_EN
D28	I2S0_SDI0	底板音频编解码控制
G26	GPIO1_D5	连接底板排针
G20	VCC_1V8_S0	

C240 0.1uf 放在主芯片背面

GND

RK3588 VCCIO3

U8H

VCCIO3 Domain

Operating Voltage=1.8V

	UART6_RX_M0	FSPI_D0_M1	SDIO_D0_M0		GMAC0_RXD2		GPIO2_A6_u
	UART6_TX_M0	FSPI_D1_M1	SDIO_D1_M0		GMAC0_RXD3		GPIO2_A7_u
I2C8_SCL_M1	UART6_RTSN_M0	FSPI_D2_M1	SDIO_D2_M0		GMAC0_RXCLK		GPIO2_B0_u
I2C8_SDA_M1	UART6_CTSN_M0	FSPI_D3_M1	SDIO_D3_M0		GMAC0_TXD2		GPIO2_B1_u
I2C3_SCL_M3			SDIO_CMD_M0		GMAC0_TXD3		GPIO2_B2_u
I2C3_SDA_M3		FSPI_CLK_M1	SDIO_CLK_M0		GMAC0_TXCLK		GPIO2_B3_d
I2C4_SDA_M1	UART7_RX_M0	FSPI_CS0N_M1	HDMI_TX1_SDA_M0		GMAC0_PTP_REFCLK		GPIO2_B4_u
I2C4_SCL_M1	UART7_TX_M0	FSPI_CS1N_M1	HDMI_TX1_SCL_M0		GMAC0_PPSTRIG		GPIO2_B5_u
I2C5_SCL_M4	UART1_RX_M0		I2S2_MCLK_M0		GMAC0_TXD0		GPIO2_B6_d
I2C5_SDA_M4	UART1_TX_M0		I2S2_SCLK_M0		GMAC0_TXD1		GPIO2_B7_d
I2C2_SDA_M1	UART1_RTSN_M0	SPI1_CLK_M0	I2S2_LRCK_M0		GMAC0_TXEN		GPIO2_C0_d
I2C2_SCL_M1	UART1_CTSN_M0	SPI1_MISO_M0			GMAC0_RXD0		GPIO2_C1_d
I2C6_SDA_M2	UART9_TX_M0	SPI1_MOSI_M0			GMAC0_RXD1		GPIO2_C2_d
I2C6_SCL_M2		SPI1_CS0_M0	I2S2_SDI_M0		ETH0_REFCLKO_25M		GPIO2_C3_d
TEST_CLKOUT_M1	UART9_RX_M0	SPI1_CS1_M0	HDMI_TX1_CEC_M0		GMAC0_PPSCLK		GPIO2_C4_d
					CLK32K_OUT1		GPIO2_C5_d
	UART7_RTSN_M0	SPI3_CS0_M0	PWM2_M2		GMAC0_RXDV_CRS		GPIO4_C2_d
I2C7_SCL_M1	PWM4_M1	SPI3_CS1_M0	I2S2_SDO_M0		GMAC0_MCLKINOUT		GPIO4_C3_d
I2C7_SDA_M1	UART9_RTSN_M0	SPI3_MISO_M0	PWM5_M2		GMAC0_MDC		GPIO4_C4_d
I2C8_SCL_M1	UART9_CTSN_M0	SPI3_MOSI_M0	PWM6_M2		GMAC0_MDIO		GPIO4_C5_d
I2C8_SDA_M1	UART7_CTSN_M0	SPI3_CLK_M0	PWM7_IR_M3		GMAC0_TXER		GPIO4_C6_d

VCCIO3_1V8

RK3588

AC32	GMAC0_RXD2		
AC31	GMAC0_RXD3		
AE32	GMAC0_RXCLK		
AC33	GMAC0_TXD2_R	R101	0R
AC34	GMAC0_TXD3_R	R102	0R
AE33	GMAC0_TXCLK_R	R111	0R
AB31	GMAC0_TXCLK		
AB30	HDMI_TX1_SDA_M0		
AD33	GMAC0_TXD0_R	R112	0R
AD34	GMAC0_TXD1_R	R113	0R
AE34	GMAC0_TXEN_R	R114	0R
AD32	GMAC0_TXEN		
AD31	GMAC0_RXD0		
AD30	GMAC0_RXD1		
AC30	HDMI_TX1_CEC_M0		HDMI控制信号
AE30	GPIO2_C5		M2PCIE_PWR_EN
AE31	GMAC0_RXDV_CRS		
AF34	GMAC0_MCLKINOUT	R115	0R
AB34	GMAC0_MDC_R	R116	0R
AB33	GMAC0_MDIO_R	R117	0R
AF33	GMAC0_MDIO		
	GPIO4_C6		PCIEx4_PWR_EN
Y26	VCC_1V8_S0		

通知GMAC有有效数据可读

MDIO接口时钟

C241 0.1uf 放在主芯片背面

GND

RK3588 SARADC

U8U

If SARADC_IN0_BOOT=0V after power-on reset, then system will enter into Maskrom mode.

SARADC

12-bit 1MS/s

SARADC_IN0_BOOT	AM16	SARADC_IN0_BOOT
Recovery/ SARADC_IN1	AL16	RECOVERY_KEY
SARADC_IN2	AK16	SARADC_IN2
SARADC_IN3	AN17	SARADC_IN3
SARADC_IN4	AM17	SARADC_IN4
SARADC_IN5	AK15	
SARADC_IN6	AL17	
SARADC_IN7	AK17	
SARADC_AVDD_1V8	AH18	VCCA_1V8_S0

C237 0.1uf 放在主芯片背面

GND

OTP

NC	AD4	
OTP_VDDOTP_0V75	AD3	VDD_0V75_S0

C239 0.1uf 放在主芯片背面

GND

TSADC

TSADC_TEST_OUT_TS	AF18	

RK3588

SARADC_IN0_BOOT	C230	1nf
RECOVERY_KEY	C231	1nf
SARADC_IN2	C232	1nf
SARADC_IN3	C233	1nf
SARADC_IN4	C234	1nf

GND

VCCA_1V8_S0

R60 10K

RECOVERY_KEY

BOARD ID

VCCA_1V8_S0

R61 1K

SARADC_IN2

R63 10K

GND

Board ID:0x06xx

电压值 : VIN2:1.636V

ADC值:VIN2:3722

VCCA_1V8_S0

R6 25.5K

SARADC_IN3

R17 10K

GND

Board ID:0x0601

电压值 : VIN3:0.507V

ADC值:VIN3:1153

BOOT MODE CONFIG

VCCA_1V8_S0

R62 100K

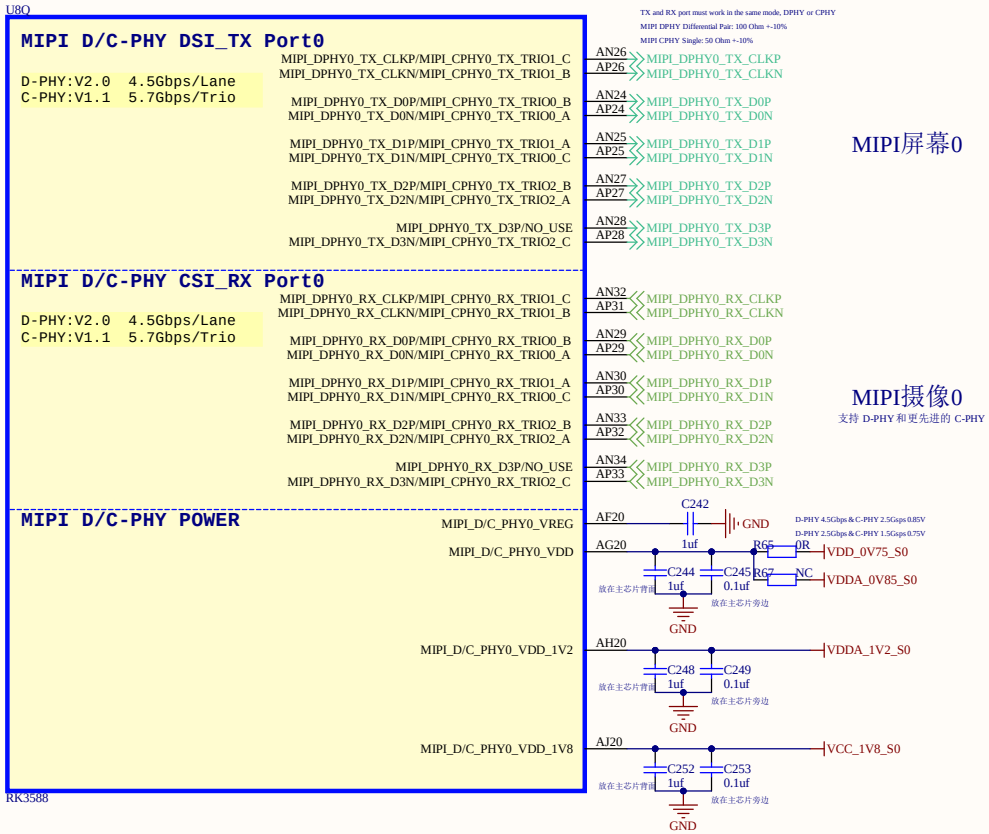
SARADC_IN0_BOOT

R64 NC

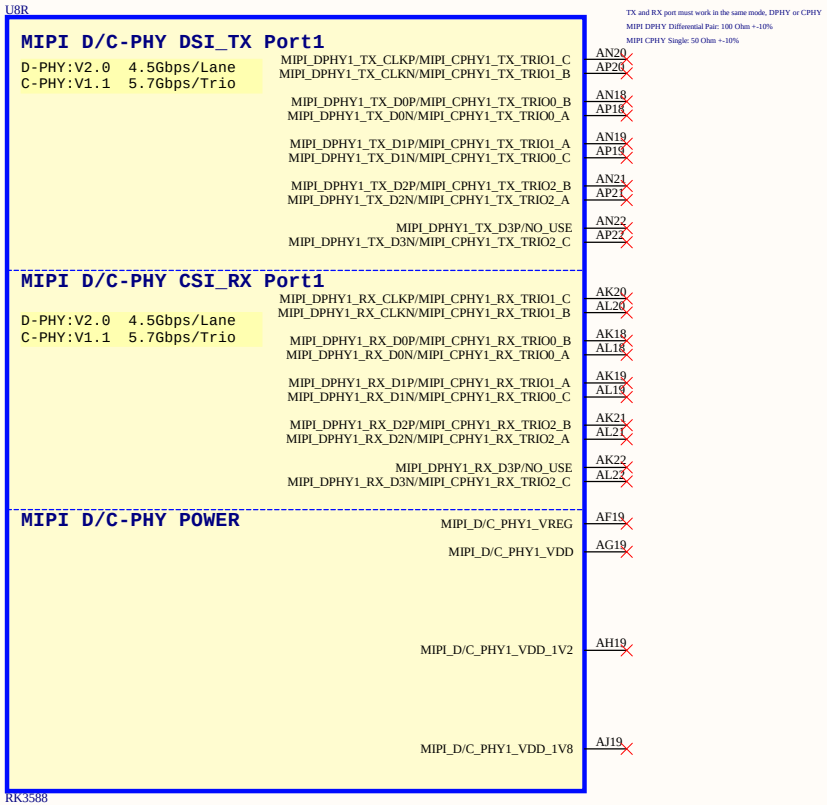
GND

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	DNP	100K	0	0V	USB (Maskrom mode)
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	100K	51K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	100K	200K	2730	1.2V	FSPI M1-USB
LEVEL6	100K	499K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB

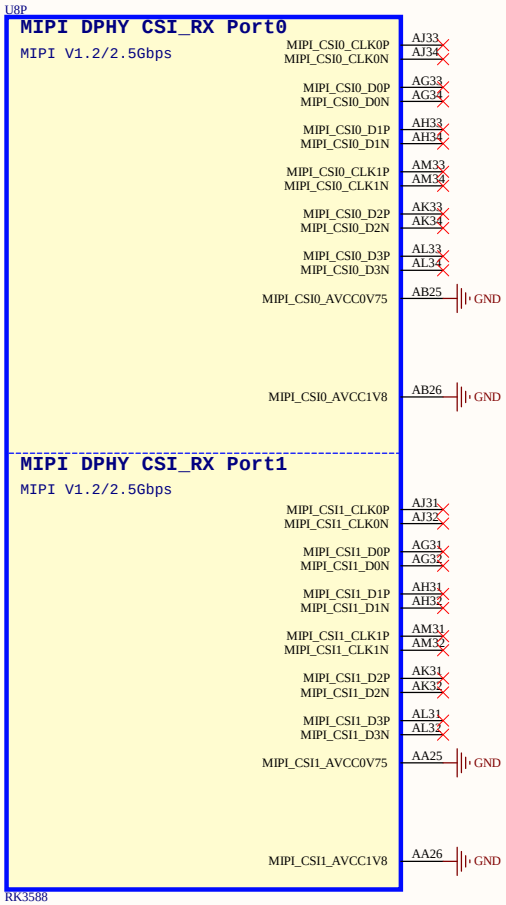
RK3588 MIPI_D/C_PHY0



RK3588 MIPI_D/C_PHY1



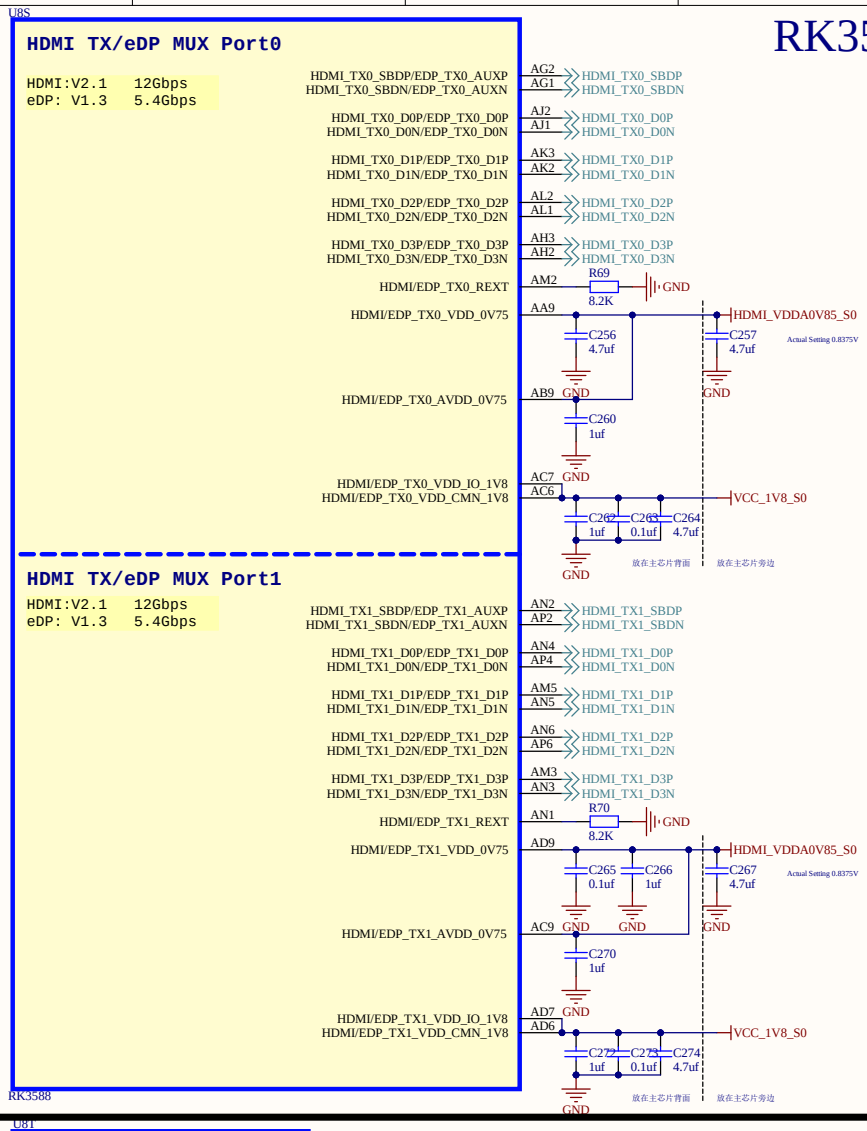
RK3588 MIPI_CSI_RX_PHY



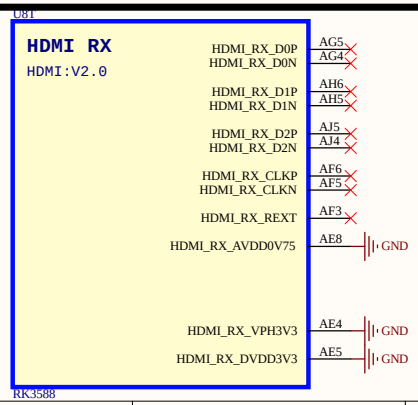
MIPI_CSI_RX Configuration

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* *+* *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0*
		MIPI_CSI_RX_D2-3 *MIPI_CSI_RX_CLK1*

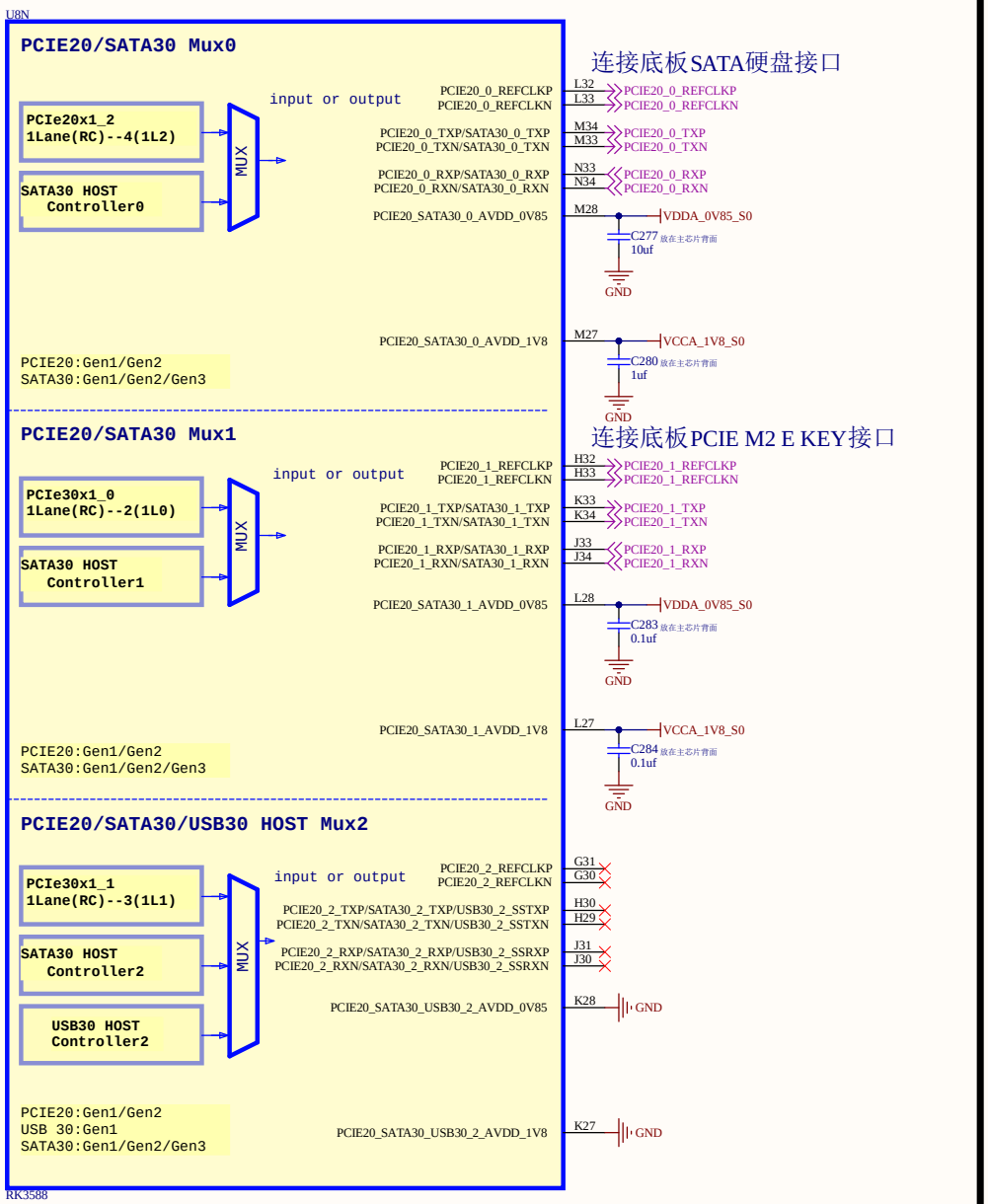
RK3588 HDMI2.1 TX



RK3588 HDMI2.0 RX



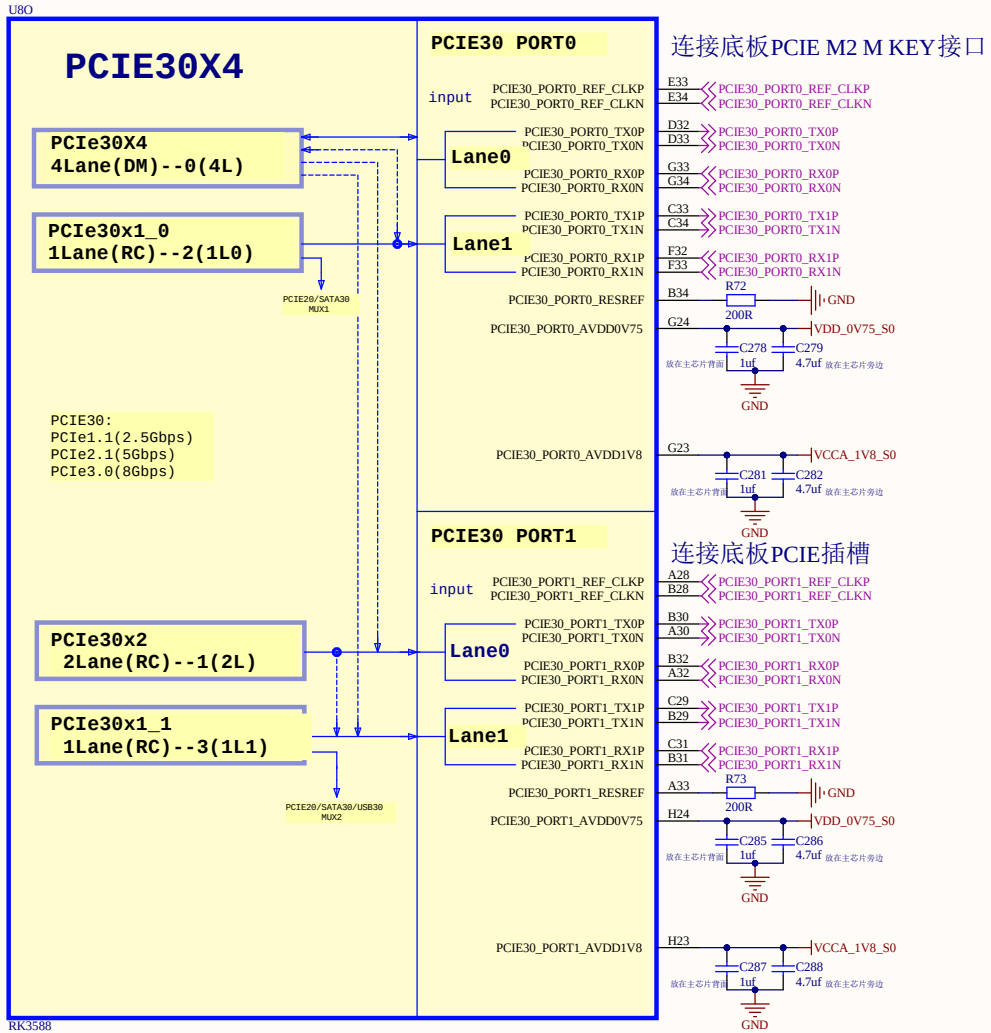
RK3588 PCIE2.0



连接底板SATA硬盘接口

连接底板PCIE M2 E KEY接口

RK3588 PCIE3.0



连接底板PCIE M2 M KEY接口

连接底板PCIE插槽

RK3588 VCCIO4

U8I

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

				/SPI4_MISO_M2	/PCIE30X1_1_CLKREQN_M2	/ DP0_HPDIN_M2	/ I2C2_SDA_M4	/ UART6_RX_M1	/ GPIO1_A0_d	A24	I2C2_SDA_M4	MIPI DSI0 LCD接口
SATA1_ACT_LED_M1	/		/	/SPI4_MOSI_M2	/PCIE30X1_1_WAKEN_M2	/ DP1_HPDIN_M2	/ I2C2_SCL_M4	/ UART6_TX_M1	/ GPIO1_A1_d	A25	I2C2_SCL_M4	MIPI DSI0 LCD接口
			/ PWM0_M2	/SPI4_CLK_M2	/	/ VOP_POST_EMPTY	/ I2C4_SDA_M3	/ UART6_RTSN_M1	/ GPIO1_A2_d	A26	GPIO1_A2	LCD0_BL_PWM
			/ PWM1_M2	/SPI4_CS0_M2	/	/ HDMI_TX1_SDA_M2	/ I2C4_SCL_M3	/ UART6_CTSN_M1	/ GPIO1_A3_d	A27		
			/	/SPI2_MISO_M0	/	/ HDMI_TX1_SCL_M2	/	/	/ GPIO1_A4_d	B25	GPIO1_A4	HDMI0_TX_ON
			/	/SPI2_MOSI_M0		/ HDMI_TX0_HPD_M0	/	/	/ GPIO1_A5_d	B26	HDMI_TX0_HPD_M0	
			/	/SPI2_CLK_M0	/	/ HDMI_TX1_HPD_M0	/	/	/ GPIO1_A6_d	C24	HDMI_TX1_HPD_M0	
			/ PWM3_IR_M3	/SPI2_CS0_M0	/PCIE30X1_1_PERSTN_M2	/	/ PDM1_SDI0_M1	/	/ GPIO1_A7_u	C25	GPIO1_A7	HDMI1_TX_ON
			/	/SPI2_CS1_M0	/PCIE30X4_CLKREQN_M3	/	/ PDM1_SDI1_M1	/	/ GPIO1_B0_u	C27	GPIO1_B0	TYPEC0_SBU1_DC
			/	/SPI0_MISO_M2	/PCIE30X4_WAKEN_M3	/	/ PDM1_SDI2_M1	/	/ GPIO1_B1_d	D25	GPIO1_B1	TYPEC0_SBU2_DC
			/	/SPI0_MOSI_M2	/PCIE30X4_PERSTN_M3	/	/ PDM1_SDI3_M1	/ UART4_RX_M2	/ GPIO1_B2_d	D26	UART4_RX_M2	UART4_RX
SATA0_ACT_LED_M1	/		/	/SPI0_CLK_M2	/PCIE30X1_0_WAKEN_M2	/	/ PDM1_CLK1_M1	/ UART4_TX_M2	/ GPIO1_B3_d	D27	UART4_TX_M2	UART4_TX
			/	/SPI0_CS0_M2	/PCIE30X1_0_PERSTN_M2	/	/ PDM1_CLK0_M1	/ UART7_RX_M2	/ GPIO1_B4_u	E24	UART7_RX_M2	UART7_RX
			/	/SPI0_CS1_M2	/PCIE30X1_0_CLKREQN_M2	/	/	/ UART7_TX_M2	/ GPIO1_B5_u	E25	UART7_TX_M2	UART7_TX
		HDMI_RX_HPDOUT_M2	/	/SPDIF0_TX_M0	/PCIE30X2_WAKEN_M3	/ MIPI_CAMERA1_CLK_M0	/ I2C5_SCL_M3	/ UART1_TX_M1	/ GPIO1_B6_u	E26	I2C5_SCL_M3	连接底板排针
SATA2_ACT_LED_M1	/	HDMI_RX_CEC_M2	/ PWM13_M2	/SPDIF1_TX_M0	/PCIE30X2_PERSTN_M3	/ MIPI_CAMERA2_CLK_M0	/ I2C5_SDA_M3	/ UART1_RX_M1	/ GPIO1_B7_u	E27	I2C5_SDA_M3	连接底板排针
		HDMI_RX_SCL_M2	/ PWM14_M2	/	/	/ MIPI_CAMERA3_CLK_M0	/ I2C8_SCL_M2	/ UART1_RTSN_M1	/ GPIO1_D6_u	F24	I2C8_SCL_M2	连接底板排针
		HDMI_RX_SDA_M2	/ PWM15_IR_M3	/	/PCIE30X2_CLKREQN_M3	/ MIPI_CAMERA4_CLK_M0	/ I2C8_SDA_M2	/ UART1_CTSN_M1	/ GPIO1_D7_u	F25	I2C8_SDA_M2	连接底板排针

VCCIO4_1V8 — H20 — VCC_1V8_S0

C291 0.1uf 放在主芯片背面 — GND

VCCIO4 — H21 — VCC_3V3_S0

C292 0.1uf 放在主芯片背面 — GND

RK3588

RK3588 VCCIO5

U8J

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM10_M0	SPI4_MISO_M1		I2C6_SDA_M4	FSPI_D0_M2	I2S3_MCLK	SDIO_D0_M1	GMAC1_TXD2	GPIO3_A0_u	AA29
AUDDSM_LN	SPI4_MOSI_M1	PWM11_IR_M0	I2C6_SCL_M4	FSPI_D1_M2	I2S3_SCLK	SDIO_D1_M1	GMAC1_TXD3	GPIO3_A1_u	AA30
AUDDSM_LP	SPI4_CLK_M1	UART8_TX_M1		FSPI_D2_M2	I2S3_LRCK	SDIO_D2_M1	GMAC1_RXD2	GPIO3_A2_u	AD27
AUDDSM_RN	SPI4_CS0_M1	UART8_RX_M1		FSPI_D3_M2	I2S3_SDO	SDIO_D3_M1	GMAC1_RXD3	GPIO3_A3_u	AE27
AUDDSM_RP	SPI4_CS1_M1	UART8_RTSN_M1			I2S3_SDI	SDIO_CMD_M1	GMAC1_TXCLK	GPIO3_A4_d	AD28
	MIPI_CAMERA0_CLK_M1	UART8_CTSN_M1	I2C4_SDA_M0	FSPI_CLK_M2		SDIO_CLK_M1	GMAC1_RXCLK	GPIO3_A5_d	AH30
	MIPI_CAMERA1_CLK_M1		I2C4_SCL_M0				ETH1_REFCLKO_25M	GPIO3_A6_d	AH27
PWM8_M0	MIPI_CAMERA2_CLK_M1						GMAC1_RXD0	GPIO3_A7_u	AG29
PWM9_M0	MIPI_CAMERA3_CLK_M1						GMAC1_RXD1	GPIO3_B0_u	AG28
PWM2_M1	MIPI_CAMERA4_CLK_M1	UART2_TX_M2					GMAC1_RXDV_CRS	GPIO3_B1_d	AH29
PWM3_IR_M1		UART2_RX_M2			I2S2_SDI_M1		GMAC1_TXER	GPIO3_B2_d	AE28
		UART2_RTSN			I2S2_SDO_M1		GMAC1_TXD0	GPIO3_B3_u	AC28
		UART2_CTSN			I2S2_MCLK_M1		GMAC1_TXD1	GPIO3_B4_u	AC29
PWM12_M0	CAN1_RX_M0	UART3_TX_M1			I2S2_SCLK_M1		GMAC1_TXEN	GPIO3_B5_u	AD29
PWM13_M0	CAN1_TX_M0	UART3_RX_M1			I2S2_LRCK_M1		GMAC1_MCLKINOUT	GPIO3_B6_d	AE29
			I2C3_SCL_M1	SPI1_MOSI_M1	HDMI_TX1_HPD_M1		GMAC1_PTP_REF_CLK	GPIO3_B7_d	AA28
		UART7_TX_M1	I2C3_SDA_M1	SPI1_MISO_M1			GMAC1_PPSTRIG	GPIO3_C0_d	Y29
	PCIE30X2_BUTTON_RSTN	UART7_RX_M1		SPI1_CLK_M1			GMAC1_PPSCLK	GPIO3_C1_d	Y27
PWM14_M0		UART7_RTSN_M1	I2C8_SCL_M4	SPI1_CS0_M1		MIPI_TE0	GMAC1_MDC	GPIO3_C2_d	Y31
PWM15_IR_M0		UART7_CTSN_M1	I2C8_SDA_M4	SPI1_CS1_M1		MIPI_TE1	GMAC1_MDIO	GPIO3_C3_d	Y30
CAN2_RX_M0	PCIE30X4_CLKREQN_M2	UART5_TX_M1	FSPI_CS0N_M2	SPI3_CS0_M3	HDMI_TX1_CEC_M2		CIF_D8	GPIO3_C4_u	AH26
CAN2_TX_M0	PCIE30X4_WAKEN_M2	UART5_RX_M1	FSPI_CS1N_M2	SPI3_CS1_M3	HDMI_TX1_SDA_M1		CIF_D9	GPIO3_C5_u	AH25
	PCIE30X4_PERSTN_M2			SPI3_MISO_M3	HDMI_TX1_SCL_M1		CIF_D10	GPIO3_C6_u	AG26
	PCIE20X1_2_CLKREQN_M0		I2C5_SCL_M0	SPI3_MOSI_M3	HDMI_TX0_SCL_M2		CIF_D11	GPIO3_C7_u	AJ24
PWM8_M2	PCIE20X1_2_WAKEN_M0	UART4_RX_M1	I2C5_SDA_M0	SPI3_CLK_M3	HDMI_TX0_SDA_M2		CIF_D12	GPIO3_D0_u	AH24
PWM9_M2	PCIE20X1_2_PERSTN_M0	UART4_TX_M1		SPI0_MISO_M3	HDMI_RX_CEC_M1		CIF_D13	GPIO3_D1_d	AG23
	PCIE30X2_CLKREQN_M2	UART9_RTSN_M2	I2C7_SCL_M2	SPI0_MOSI_M3	HDMI_RX_SCL_M1		CIF_D14	GPIO3_D2_d	AG25
PWM10_M2	PCIE30X2_WAKEN_M2	UART9_CTSN_M2	I2C7_SDA_M2	SPI0_CLK_M3	HDMI_RX_SDA_M1		CIF_D15	GPIO3_D3_d	AG24
	PCIE30X2_PERSTN_M2	UART9_RX_M2		SPI0_CS0_M3	HDMI_RX_HPDOUT_M1	HDMI_TX0_HPD_M1	MCU_JTAG_TCK_M1	GPIO3_D4_d	AA27
PWM11_IR_M3	PCIE30X4_BUTTON_RSTN	UART9_TX_M2		SPI0_CS1_M3	DP1_HPDIN_M0		MCU_JTAG_TMS_M1	GPIO3_D5_d	AB28

RK3588

GPIO3_A6 — 连接底板排针

GPIO3_B2 — CTP0_INT

GPIO3_C0 — GMAC0_RSTn

GPIO3_D5 — SPK_CTRL

VCCIO5_1V8 — W25 — VCC_1V8_S0 — C293 0.1uf 放在主芯片背面 — GND

VCCIO5 — W26 — VCC_3V3_S0 — C294 0.1uf 放在主芯片背面 — GND

RK3588 VCCIO6

U8K

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

		SPI0_MISO_M1	UART9_RTSN_M1		I2S1_MCLK_M0	PCIE30X1_1_CLKREQN_M1	BT1120_D0	CIF_D0	GPIO4_A0_d	AK30		
		SPI0_MOSI_M1	UART9_CTSN_M1		I2S1_SCLK_M0	PCIE30X1_1_WAKEN_M1	BT1120_D1	CIF_D1	GPIO4_A1_d	AL30		
		SPI0_CLK_M1			I2S1_LRCK_M0	PCIE30X1_1_PERSTN_M1	BT1120_D2	CIF_D2	GPIO4_A2_d	AM29		
			UART0_TX_M2			PCIE30X1_0_CLKREQN_M1	BT1120_D3	CIF_D3	GPIO4_A3_d	AL29	GPIO4_A3	TYPEC_VBUS_EN
		SPI2_MISO_M1	UART0_RX_M2	I2C3_SCL_M2		PCIE30X1_0_WAKEN_M1	BT1120_D4	CIF_D4	GPIO4_A4_d	AL28		
		SPI2_MOSI_M1	UART3_TX_M2	I2C3_SDA_M2	I2S1_SDI0_M0	PCIE30X1_0_PERSTN_M1	BT1120_D5	CIF_D5	GPIO4_A5_d	AK27		
		SPI2_CLK_M1	UART3_RX_M2	I2C5_SCL_M2	I2S1_SDI1_M0	PCIE30X2_CLKREQN_M1	BT1120_D6	CIF_D6	GPIO4_A6_d	AL27	PCIE30X2_CLKREQN_M1	
		SPI2_CS0_M1		I2C5_SDA_M2	I2S1_SDI2_M0	PCIE30X2_WAKEN_M1	BT1120_D7	CIF_D7	GPIO4_A7_d	AM27	PCIE30X2_WAKEN_M1	
		SPI2_CS1_M1	UART8_TX_M0	I2C6_SDA_M3	I2S1_SDI3_M0	PCIE30X2_PERSTN_M1	BT1120_CLKOUT	CIF_CLKIN	GPIO4_B0_d	AK26	PCIE30X2_PERSTN_M1	
SATA2_ACT_LED_M0	SPDIF1_TX_M1	SPI0_CS1_M1	UART8_RX_M0	I2C6_SCL_M3	I2S1_SDO0_M0	PCIE30X1_0_BUTTON_RSTN		MIPI_CAMERA0_CLK_M0	GPIO4_B1_u	AL24	GPIO4_B1	PCIE30X2_PRSNTn
CAN1_RX_M1	PWM14_M1	SPI0_CS0_M1	UART8_RTSN_M0	I2C7_SCL_M3	I2S1_SDO1_M0	PCIE30X1_1_BUTTON_RSTN	BT1120_D8	CIF_HREF	GPIO4_B2_u	AK25		
CAN1_TX_M1	PWM15_IR_M1		UART8_CTSN_M0	I2C7_SDA_M3	I2S1_SDO2_M0	PCIE20X1_2_BUTTON_RSTN	BT1120_D9	CIF_VSYNC	GPIO4_B3_u	AM25		
SPDIF0_TX_M1	PWM11_IR_M1	DP0_HPDIN_M0	UART9_TX_M1		I2S1_SDO3_M0	PCIE30X4_CLKREQN_M1	BT1120_D10	CIF_CLKOUT	GPIO4_B4_u	AL26	PCIE30X4_CLKREQN_M1	
SATA1_ACT_LED_M0	PWM12_M1	SPI3_MISO_M1	UART9_RX_M1		HDMI_RX_CEC_M0	PCIE30X4_WAKEN_M1	BT1120_D11		GPIO4_B5_d	AJ26	PCIE30X4_WAKEN_M1	
SATA0_ACT_LED_M0	PWM13_M1	SPI3_MOSI_M1		I2C5_SCL_M1	HDMI_RX_HPDOUT_M0	PCIE30X4_PERSTN_M1	BT1120_D12		GPIO4_B6_d	AJ27	PCIE30X4_PERSTN_M1	
		SPI3_CLK_M1		I2C5_SDA_M1	HDMI_TX0_SCL_M0	PCIE20X1_2_CLKREQN_M1	BT1120_D13		GPIO4_B7_u	AJ28	HDMI_TX0_SCL_M0	
		SPI3_CS0_M1		I2C8_SCL_M3	HDMI_TX0_SDA_M0	PCIE20X1_2_WAKEN_M1	BT1120_D14		GPIO4_C0_u	AJ25	HDMI_TX0_SDA_M0	
SPDIF1_TX_M2	PWM6_M1	SPI3_CS1_M1		I2C8_SDA_M3	HDMI_TX0_CEC_M0	PCIE20X1_2_PERSTN_M1	BT1120_D15		GPIO4_C1_d	AK24	HDMI_TX0_CEC_M0	

VCCIO6_1V8 — AC25 — VCC_1V8_S0

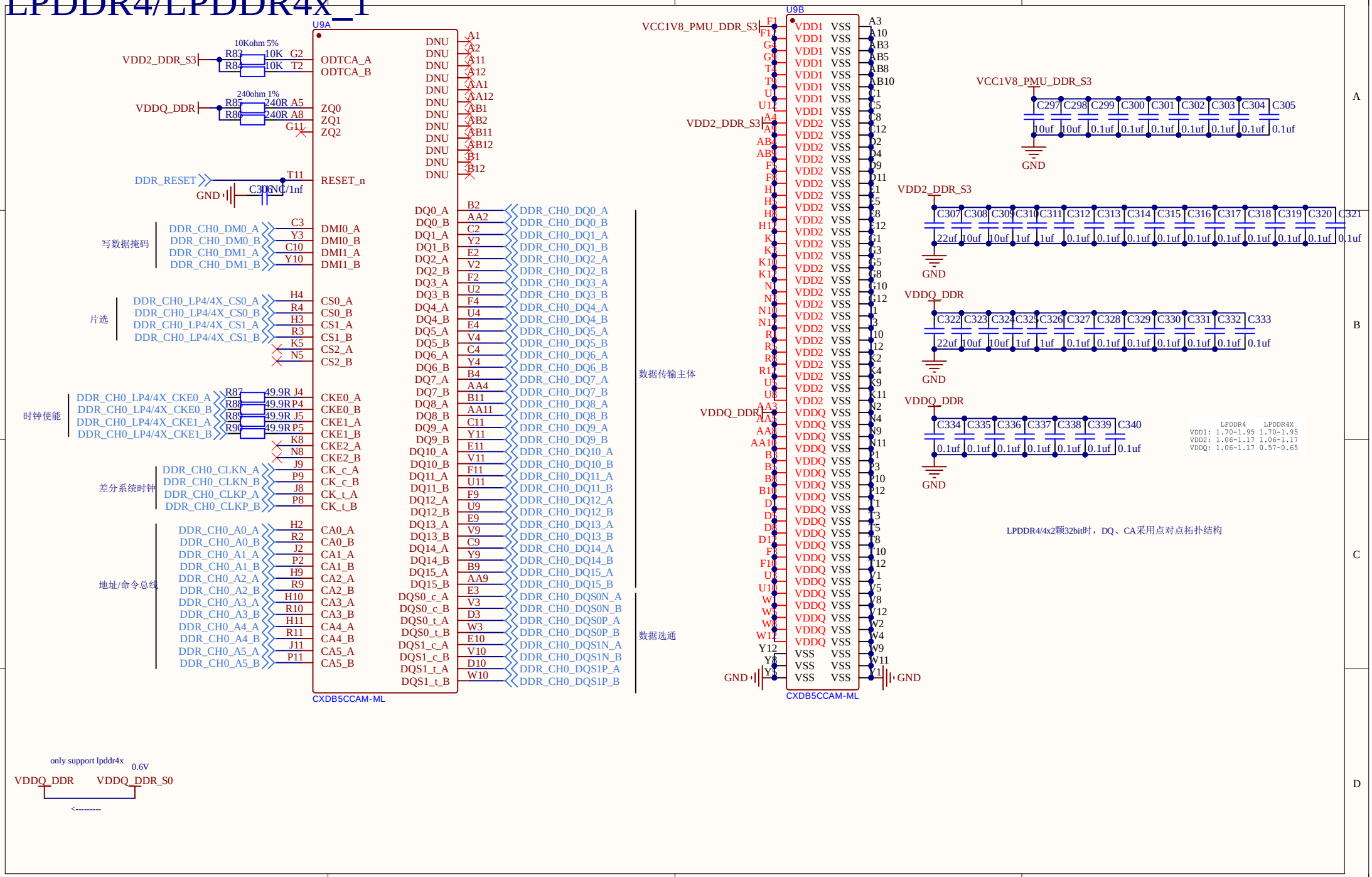
C295 放在主芯片背面 0.1uf — GND

VCCIO6 — AC26 — VCC_3V3_S0

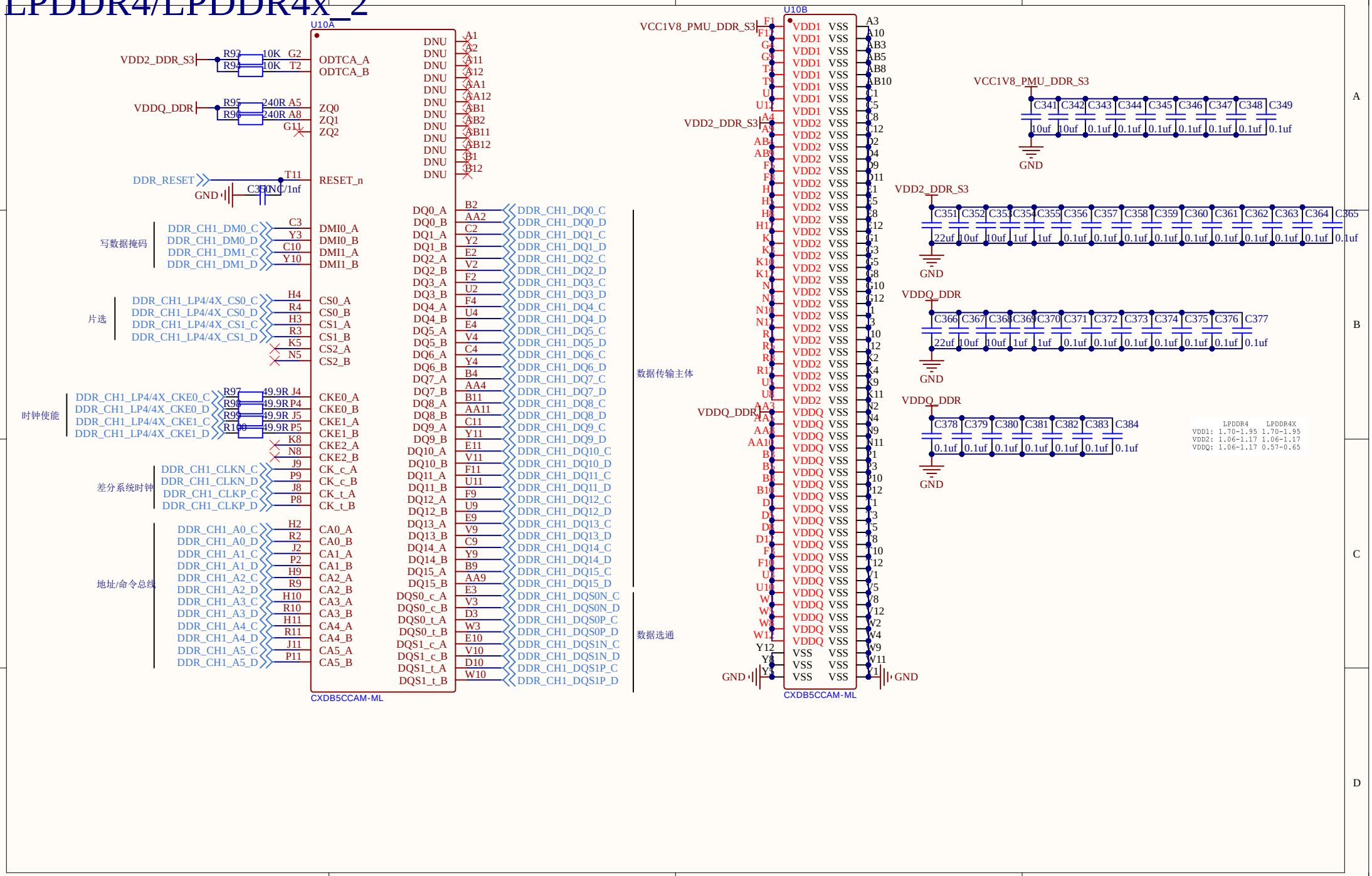
C296 放在主芯片背面 0.1uf — GND

RK3588

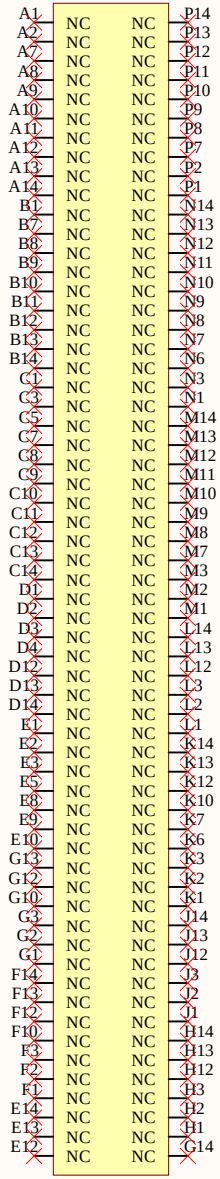
LPDDR4/LPDDR4x_1

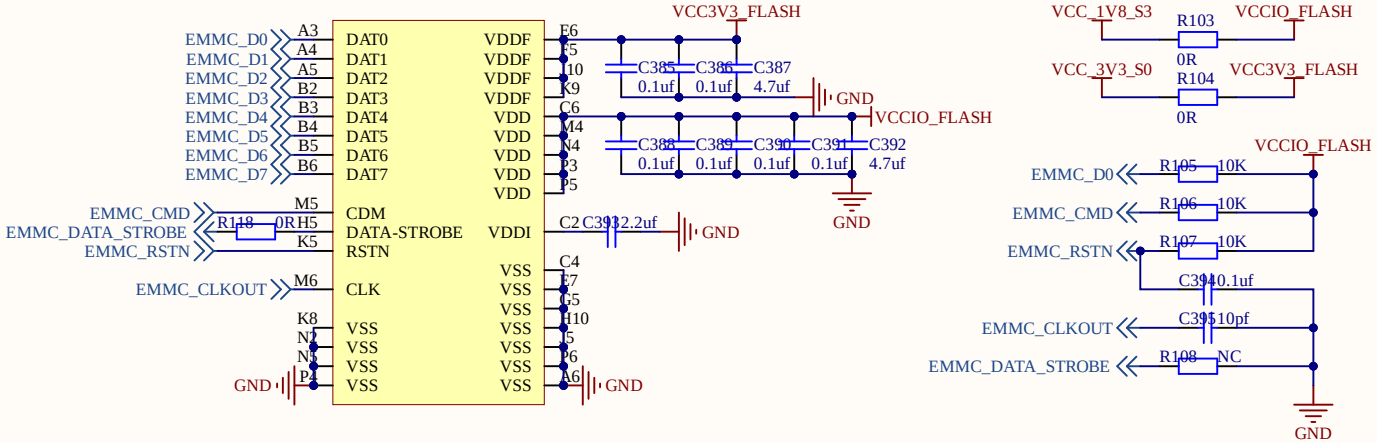


LPDDR4/LPDDR4x_2

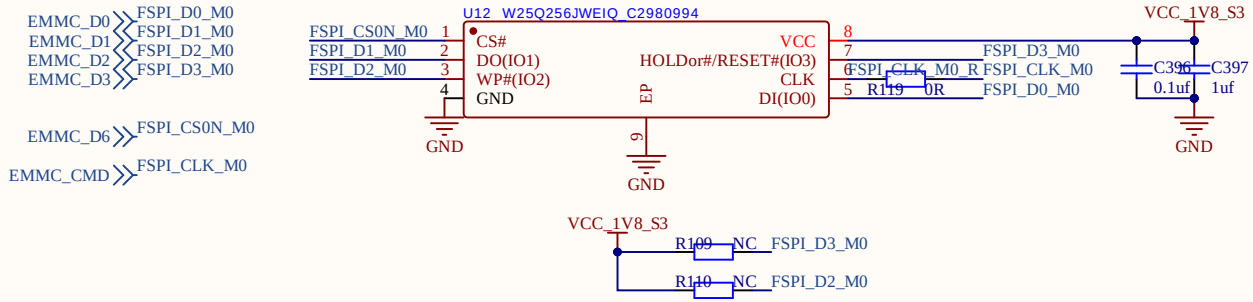


EMMC

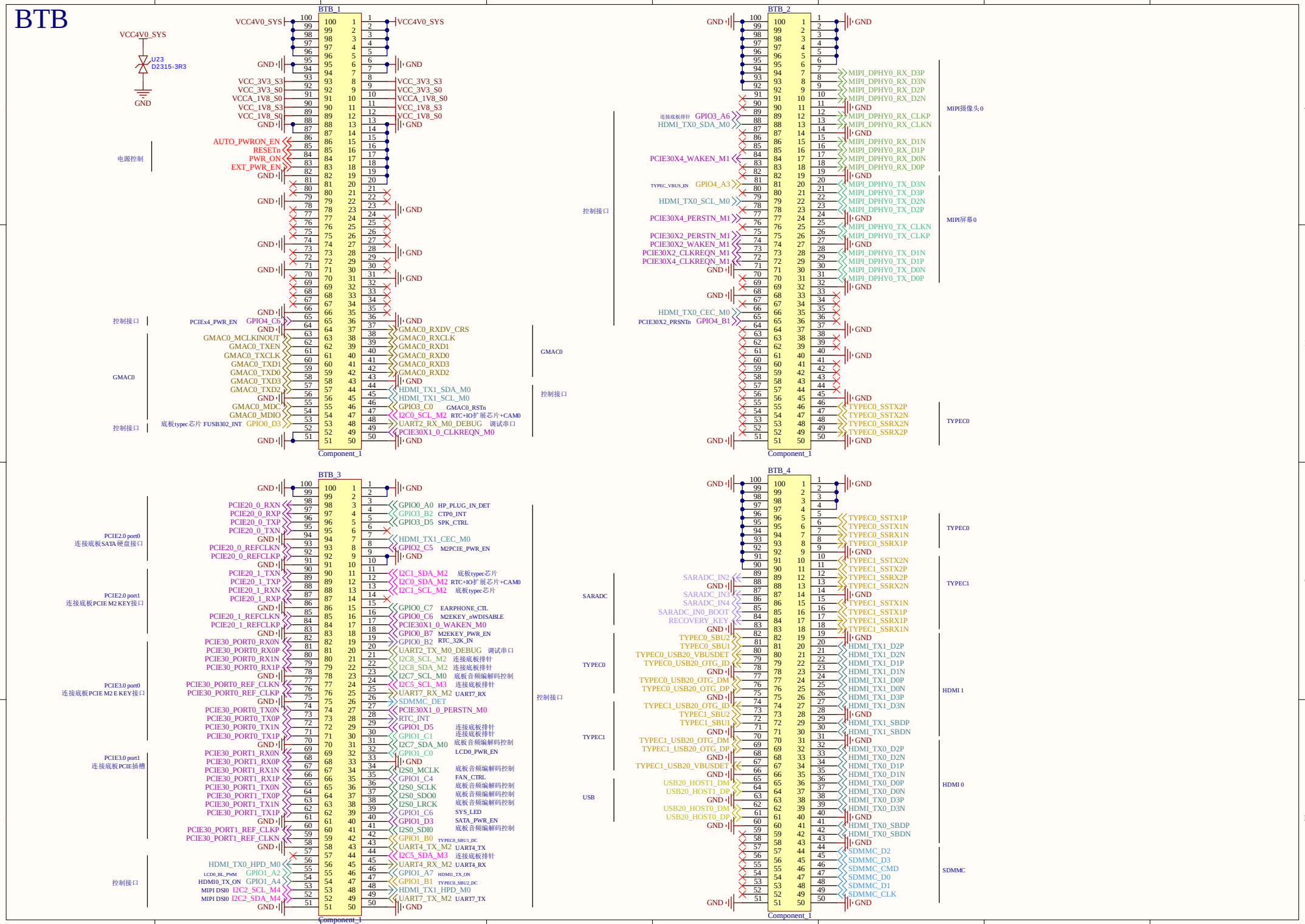




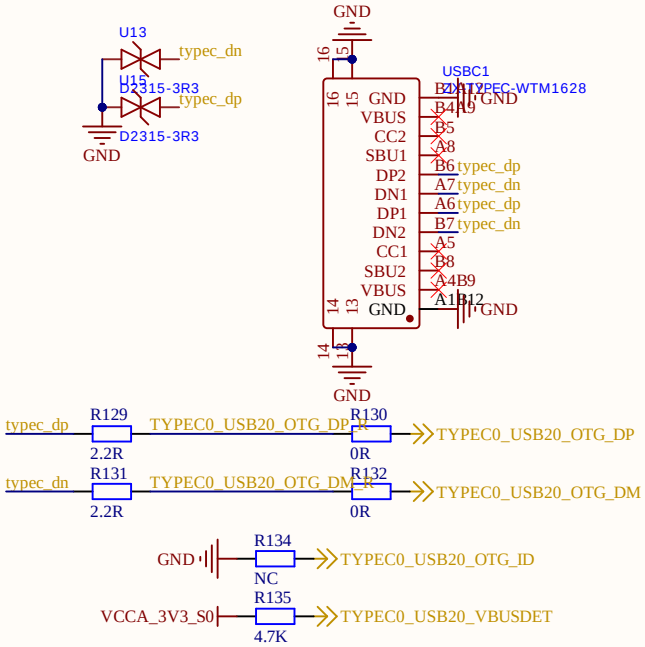
SPI Flash



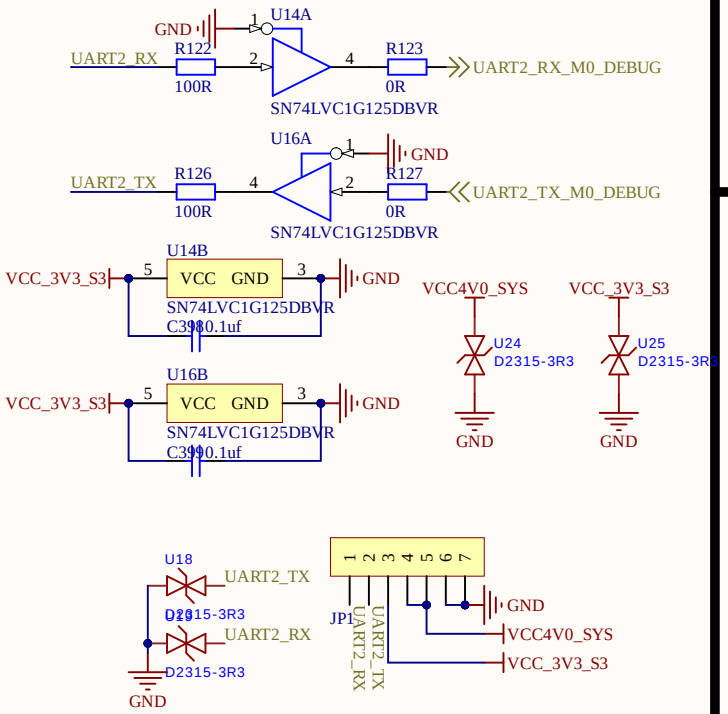
BTB


VCC4V0_SYS
U23
D2315-3R3
GND
BTB_1
Component_1
电源控制
AUTO_PWRON_EN
RESETn
PWR_ON
EXT_PWR_EN
VCC_3V3_S3
VCC_3V3_S0
VCCA_1V8_S0
VCC_1V8_S3
VCC_1V8_S0
控制接口
PCIEx4_PWR_EN GPIO4_C6
GMAC0
GMAC0_MCLKINOUT
GMAC0_TXEN
GMAC0_TXCLK
GMAC0_TXD1
GMAC0_TXD0
GMAC0_TXD3
GMAC0_TXD2
GMAC0_MDC
GMAC0_MDIO
底板typec芯片 FUSB302_INT GPIO0_D3
GMAC0_RXDV_CRS
GMAC0_RXCLK
GMAC0_RXD1
GMAC0_RXD0
GMAC0_RXD3
GMAC0_RXD2
HDMI_TX1_SDA_M0
HDMI_TX1_SCL_M0
GPIO3_C0 GMAC0_RSTn
I2C0_SCL_M2 RTC+IO扩展芯片+CAM0
UART2_RX_M0_DEBUG 调试串口
PCIE30X1_0_CLKREQN_M0
BTB_2
连接底板排针 GPIO3_A6
HDMI_TX0_SDA_M0
PCIE30X4_WAKEN_M1
TYPEC_VBUS_EN GPIO4_A3
HDMI_TX0_SCL_M0
PCIE30X4_PERSTN_M1
PCIE30X2_PERSTN_M1
PCIE30X2_WAKEN_M1
PCIE30X2_CLKREQN_M1
PCIE30X4_CLKREQN_M1
HDMI_TX0_CEC_M0
PCIE30X2_PRSNTn GPIO4_B1
MIPI_DPHY0_RX_D3P
MIPI_DPHY0_RX_D3N
MIPI_DPHY0_RX_D2P
MIPI_DPHY0_RX_D2N
MIPI_DPHY0_RX_CLKP
MIPI_DPHY0_RX_CLKN
MIPI_DPHY0_RX_D1N
MIPI_DPHY0_RX_D1P
MIPI_DPHY0_RX_D0N
MIPI_DPHY0_RX_D0P
MIPI摄像头0
MIPI_DPHY0_TX_D3N
MIPI_DPHY0_TX_D3P
MIPI_DPHY0_TX_D2N
MIPI_DPHY0_TX_D2P
MIPI_DPHY0_TX_CLKN
MIPI_DPHY0_TX_CLKP
MIPI_DPHY0_TX_D1N
MIPI_DPHY0_TX_D1P
MIPI_DPHY0_TX_D0N
MIPI_DPHY0_TX_D0P
MIPI屏幕0
TYPEC0_SSTX2P
TYPEC0_SSTX2N
TYPEC0_SSRX2N
TYPEC0_SSRX2P
TYPEC0
BTB_3
PCIE2.0 port0
连接底板SATA硬盘接口
PCIE20_0_RXN
PCIE20_0_RXP
PCIE20_0_TXP
PCIE20_0_TXN
PCIE20_0_REFCLKN
PCIE20_0_REFCLKP
PCIE2.0 port1
连接底板PCIE M2 KEY接口
PCIE20_1_TXN
PCIE20_1_TXP
PCIE20_1_RXN
PCIE20_1_RXP
PCIE20_1_REFCLKN
PCIE20_1_REFCLKP
PCIE3.0 port0
连接底板PCIE M2 E KEY接口
PCIE30_PORT0_RX0N
PCIE30_PORT0_RX0P
PCIE30_PORT0_RX1N
PCIE30_PORT0_RX1P
PCIE30_PORT0_REF_CLKN
PCIE30_PORT0_REF_CLKP
PCIE30_PORT0_TX0N
PCIE30_PORT0_TX0P
PCIE30_PORT0_TX1N
PCIE30_PORT0_TX1P
PCIE3.0 port1
连接底板PCIE插槽
PCIE30_PORT1_RX0N
PCIE30_PORT1_RX0P
PCIE30_PORT1_RX1N
PCIE30_PORT1_RX1P
PCIE30_PORT1_TX0N
PCIE30_PORT1_TX0P
PCIE30_PORT1_TX1N
PCIE30_PORT1_TX1P
PCIE30_PORT1_REF_CLKP
PCIE30_PORT1_REF_CLKN
HDMI_TX0_HPD_M0
LCD0_BL_PWM GPIO1_A2
HDMI0_TX_ON GPIO1_A4
MIPI DSI0 I2C2_SCL_M4
MIPI DSI0 I2C2_SDA_M4
GPIO0_A0 HP_PLUG_IN_DET
GPIO3_B2 CTP0_INT
GPIO3_D5 SPK_CTRL
HDMI_TX1_CEC_M0
GPIO2_C5 M2PCIE_PWR_EN
I2C1_SDA_M2 底板typec芯片
I2C0_SDA_M2 RTC+IO扩展芯片+CAM0
I2C1_SCL_M2 底板typec芯片
GPIO0_C7 EARPHONE_CTL
GPIO0_C6 M2EKEY_nWDISABLE
PCIE30X1_0_WAKEN_M0
GPIO0_B7 M2EKEY_PWR_EN
GPIO0_B2 RTC_32K_IN
UART2_TX_M0_DEBUG 调试串口
I2C8_SCL_M2 连接底板排针
I2C8_SDA_M2 连接底板排针
I2C7_SCL_M0 底板音频编解码控制
I2C5_SCL_M3 连接底板排针
UART7_RX_M2 UART7_RX
SDMMC_DET
PCIE30X1_0_PERSTN_M0
RTC_INT
GPIO1_D5 连接底板排针
GPIO1_C1 连接底板排针
I2C7_SDA_M0 底板音频编解码控制
GPIO1_C0 LCD0_PWR_EN
I2S0_MCLK 底板音频编解码控制
GPIO1_C4 FAN_CTRL
I2S0_SCLK 底板音频编解码控制
I2S0_SDO0 底板音频编解码控制
I2S0_LRCK 底板音频编解码控制
GPIO1_C6 SYS_LED
GPIO1_D3 SATA_PWR_EN
I2S0_SDI0 底板音频编解码控制
GPIO1_B0 TYPEC0_SBU1_DC
UART4_TX_M2 UART4_TX
I2C5_SDA_M3 连接底板排针
UART4_RX_M2 UART4_RX
GPIO1_A7 HDMI1_TX_ON
GPIO1_B1 TYPEC0_SBU2_DC
HDMI_TX1_HPD_M0
UART7_TX_M2 UART7_TX
BTB_4
SARADC
SARADC_IN2
SARADC_IN3
SARADC_IN4
SARADC_IN0_BOOT
RECOVERY_KEY
TYPEC0
TYPEC0_SBU2
TYPEC0_SBU1
TYPEC0_USB20_VBUSDET
TYPEC0_USB20_OTG_ID
TYPEC0_USB20_OTG_DM
TYPEC0_USB20_OTG_DP
TYPEC1
TYPEC1_USB20_OTG_ID
TYPEC1_SBU2
TYPEC1_SBU1
TYPEC1_USB20_OTG_DM
TYPEC1_USB20_OTG_DP
TYPEC1_USB20_VBUSDET
USB
USB20_HOST1_DM
USB20_HOST1_DP
USB20_HOST0_DM
USB20_HOST0_DP
TYPEC0_SSTX1P
TYPEC0_SSTX1N
TYPEC0_SSRX1N
TYPEC0_SSRX1P
TYPEC1_SSTX2N
TYPEC1_SSTX2P
TYPEC1_SSRX2P
TYPEC1_SSRX2N
TYPEC1_SSTX1N
TYPEC1_SSTX1P
TYPEC1_SSRX1P
TYPEC1_SSRX1N
HDMI_TX1_D2P
HDMI_TX1_D2N
HDMI_TX1_D1P
HDMI_TX1_D1N
HDMI_TX1_D0P
HDMI_TX1_D0N
HDMI_TX1_D3P
HDMI_TX1_D3N
HDMI_TX1_SBDP
HDMI_TX1_SBDN
HDMI 1
HDMI_TX0_D2P
HDMI_TX0_D2N
HDMI_TX0_D1P
HDMI_TX0_D1N
HDMI_TX0_D0P
HDMI_TX0_D0N
HDMI_TX0_D3P
HDMI_TX0_D3N
HDMI_TX0_SBDP
HDMI_TX0_SBDN
HDMI 0
SDMMC_D2
SDMMC_D3
SDMMC_CMD
SDMMC_D0
SDMMC_D1
SDMMC_CLK
SDMMC

DOWNLOAD

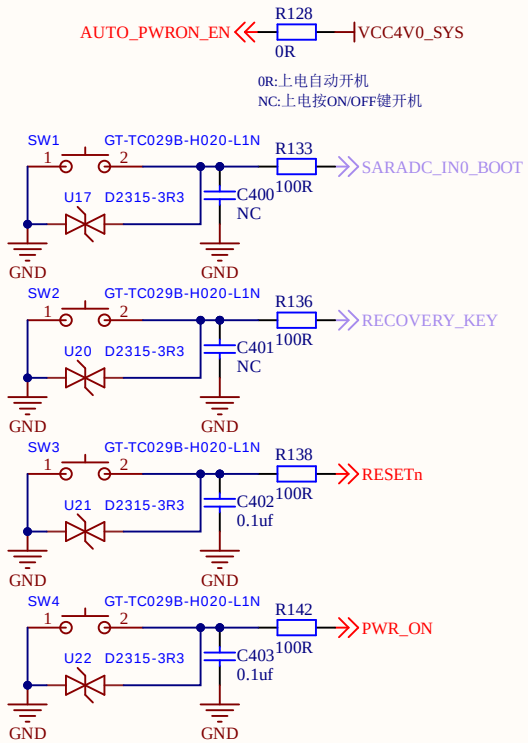


UART

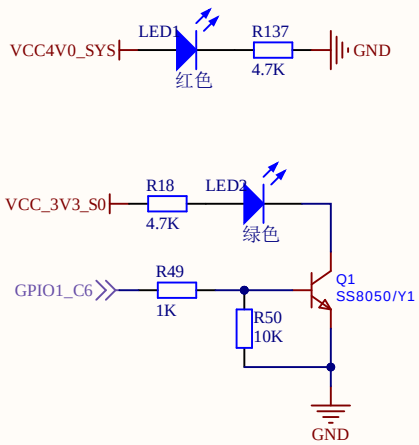
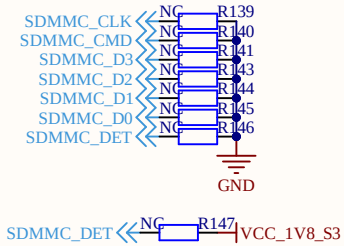


PCIE CONFIG

BOOT CONFIG



LED



SD CONFIG